

01. Block Diagram
02. System Setting
03. AM4_PCIE/Display/SVI2/JTAG
04. AM4_DDR4
05. AM4_ACPI/AZ/SD/I2C/GPIO/SMB
06. AM4_CLK/LPC/SPI/USB

08. AM4_GND
09. AM4_PWR
10. AM4_Power_CAP
11. U3SSP_repeater
12. Type_C_conn

14. DIM_DDR4 SO-DIMM A(0) BOT
15. DIM_DDR4 SO-DIMM B(0) BOT
18. DIM_CA/DQ Voltage

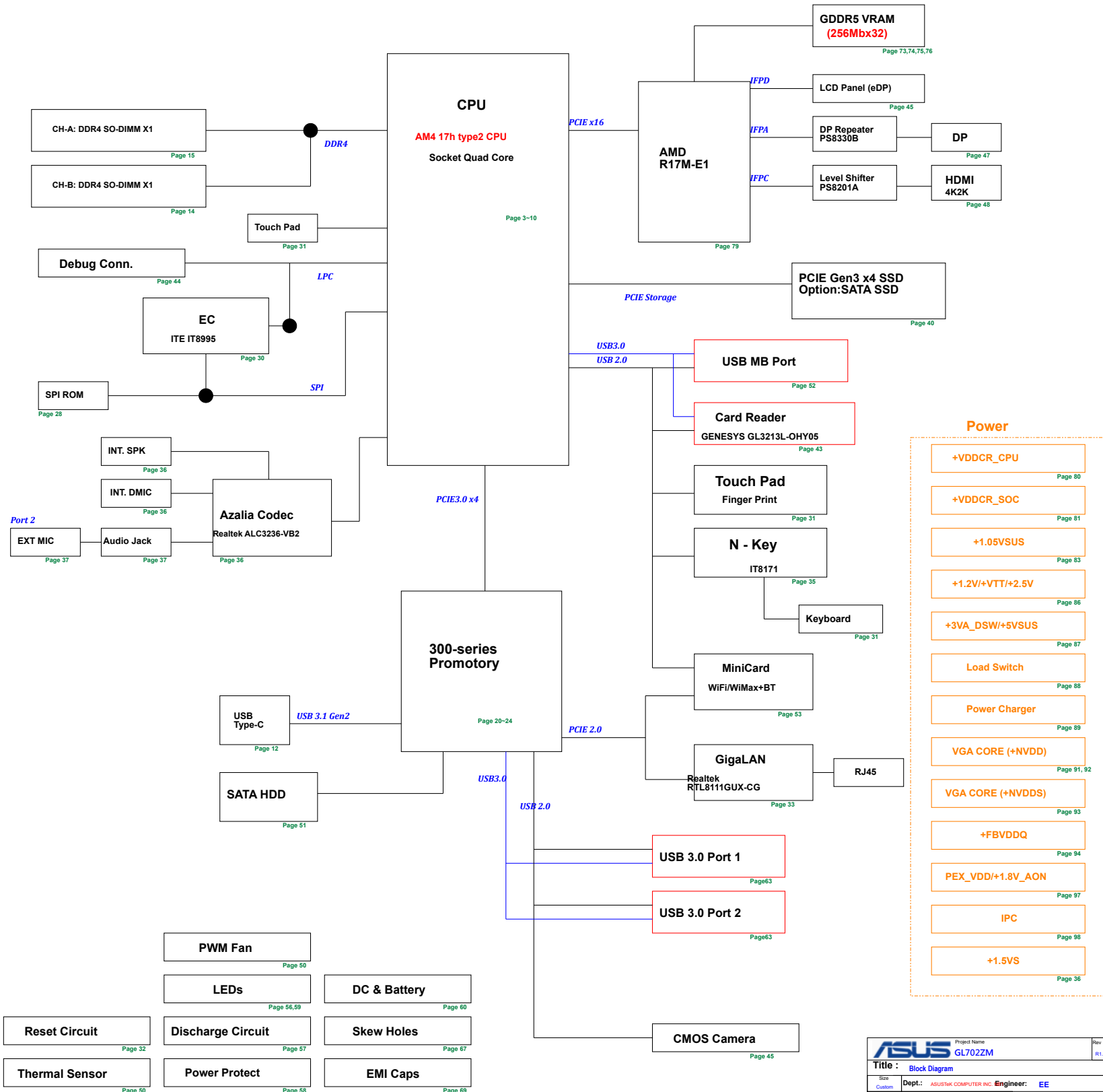
20. PROM_ACPI/SPI/GPIO/MISC/CLK
21. PROMONTORY_PCIE/SATA/SATAE
22. PROMONTORY_USB2/USB3
23. PROMONTORY_POWER
24. PROMONTORY_GND

28. SPI ROM/OTH

30. KBC_IT8995
31. KBC_KBC/KB&TP
32. RST_Reset Circuit
33. LAN_RTL8111GUX-CG
34. LAN_RJ45 CON
35. N_KEY_IT8171
36. AUD-ALC3236-CG
37. AUD-INT SPK&MIC
38.
39.
40. NGFF SSD
42.

43. CB_CON
44. DEBUG_LPC
45. CRT_eDP
47. Display Port
48. HDMI
50. FAN_Thermal Sensor&Fan
51. HDD
52. USB charger
53. Wifi/WiMax
56. LED & CON
57. DSG_Discharge
58. Power Protect
59. LED_I/O_Conn
60. DC&BAT_IN
63. USB_Port
67. screw_hole
69. OTH_EMI Caps
70. GPU_PCIE I/F
71. GPU_POWER
72. GPU_FRAME BUFFER
73. VRAM-CHANNEL A
74. VRAM-CHANNEL B
75. VRAM-CHANNEL C
76. VRAM-CHANNEL D
77. VRAM-CAP
78. GPU_CLOCK/STRAP/GPIO
79. GPU_DP/EDP/HDMI/LVDS/CRT
80. FW_IMVP8 (1)
81. FW_KABYLAKE (2)=>4+0+1
83. FW_+1.05VSUS
86. FW_1.2V/+VTT/2.5V
87. FW_+3VADSW/+5VSUS
88. FW_LOAD Switch
89. PW_CHARGER
90. PW_PROTECTION
91. PW_+NVVDD (1)
92. PW_+NVVDD (2)
93. PW_+NVVDDS
94. PW_+FBVDDQ
97. PW_+1.8VSUS
98. PW_IPC
99. PW_FLOW CHART
100. Power On Timing--AC mode
101. Power On Timing--DC mode
102. History

GL702ZC Block Diagram





Project Name

GL702ZM

Rev

R1.0

Title : <Title>

Size

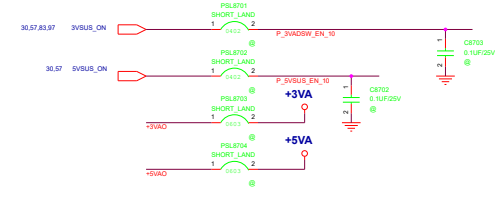
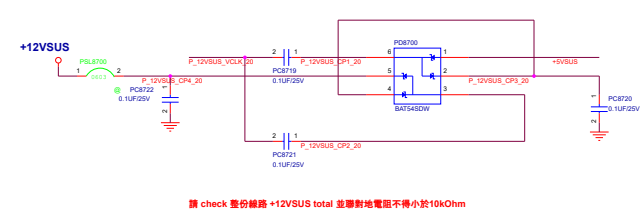
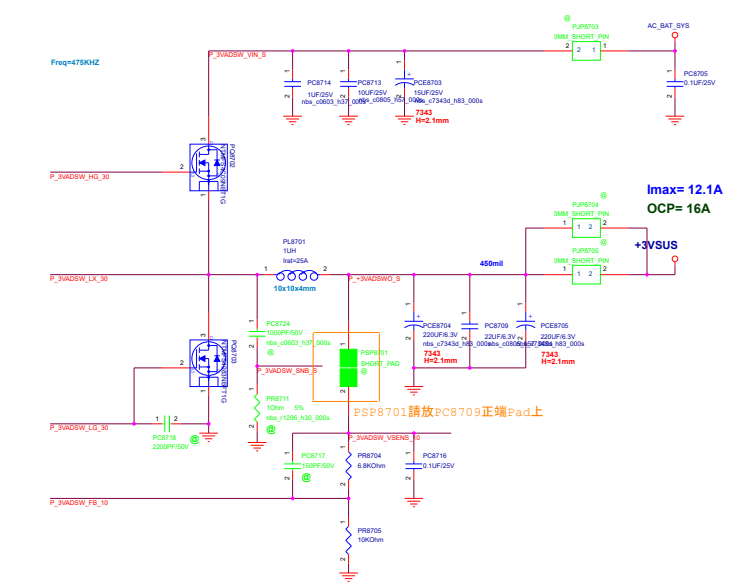
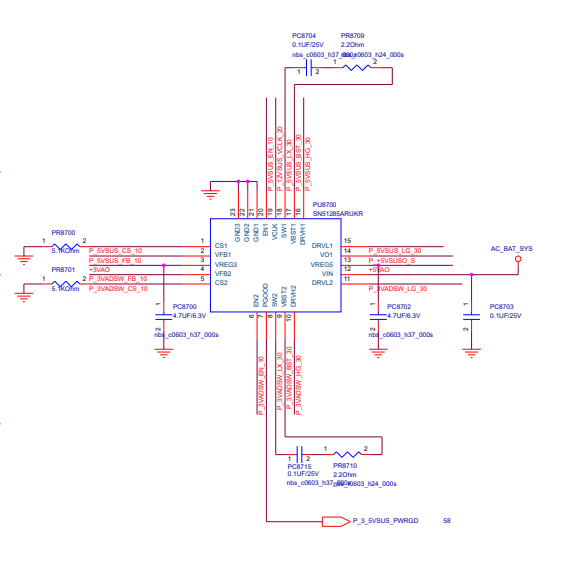
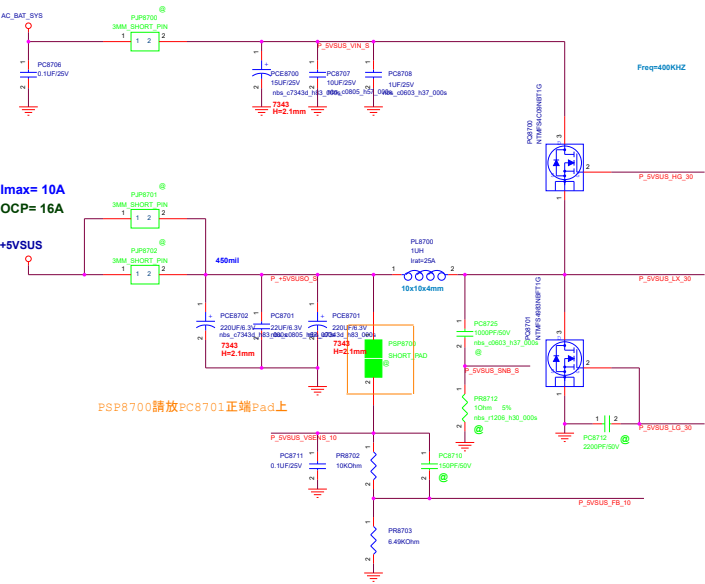
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Dept.: ASUSTeK COMPUTER INC. NB1 **Engineer:** EE

Date: Thursday, June 15, 2017

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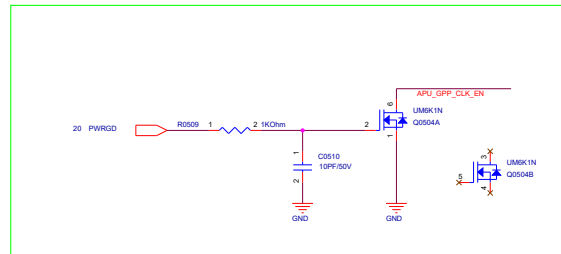
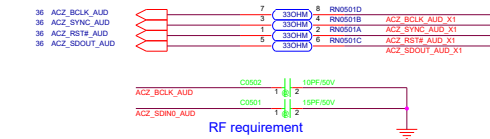
+3VA_DSW / +5VSUS [Power Power]



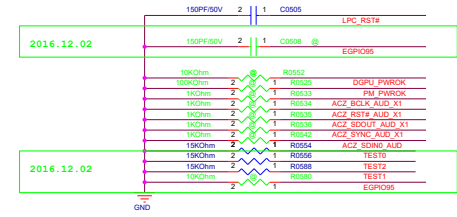
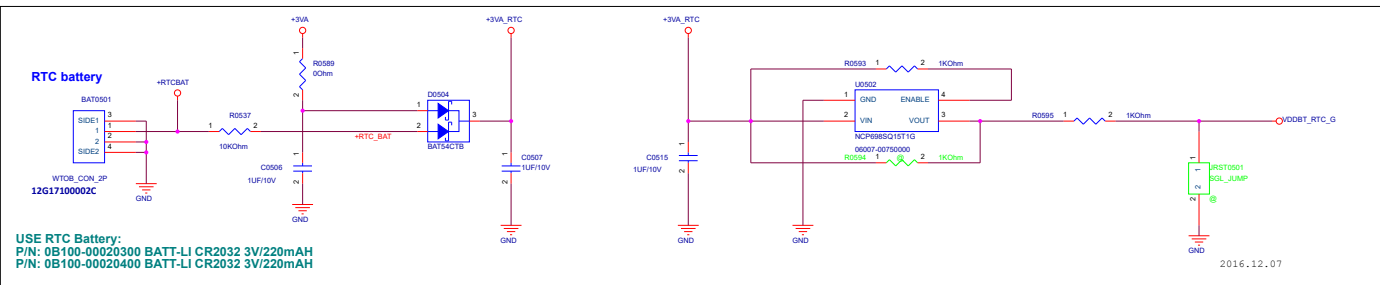
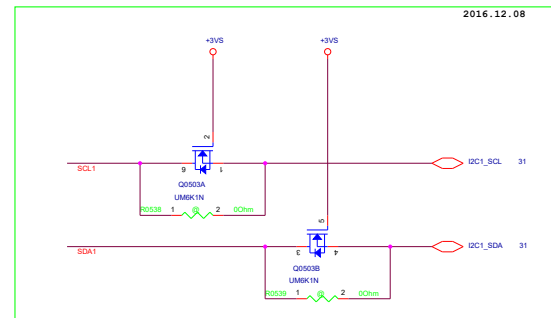
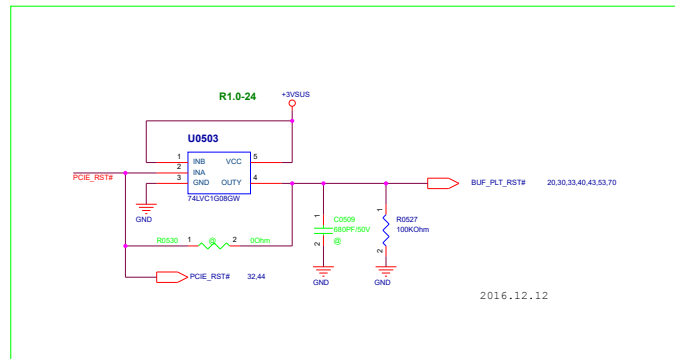
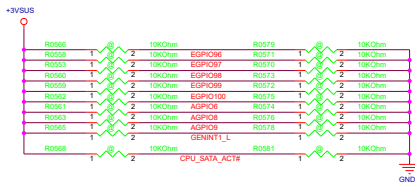
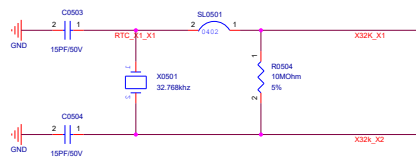
請 check 整份線路 +12VSUS total 並聯對地電阻不得小於10kOhm

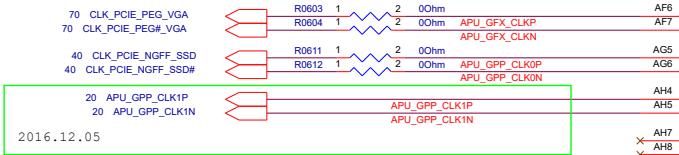
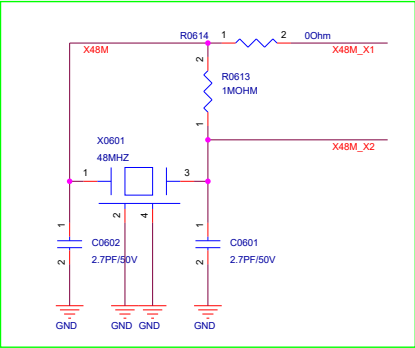
Adaptor Mode (MVP6)									
PS_ON	S0	S3	S4	S5	S6	S7	S8	S9	S10
PS_ON	1	-	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1	-	1
5VSUS_ON	1	-	1	-	0	-	0	-	0
5VSUS_ON	1	-	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0	-	0
SUSC_EC#	1	-	0	-	0	-	0	-	0

Battery Mode (MVP6)									
PS_ON	S0	S3	S4	S5	S6	S7	S8	S9	S10
PS_ON	1	-	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1	-	1
5VSUS_ON	1	-	1	-	0	-	0	-	0
5VSUS_ON	1	-	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0	-	0
SUSC_EC#	1	-	0	-	0	-	0	-	0

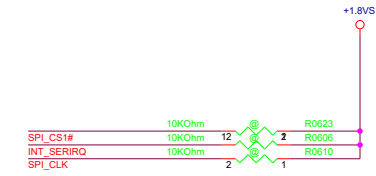


RTC CRYSTAL 32.768KHz

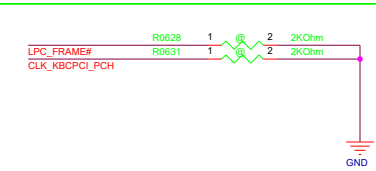




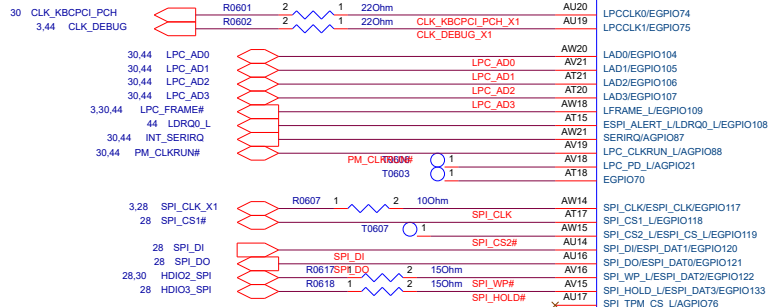
2016.12.05



2016.12.02

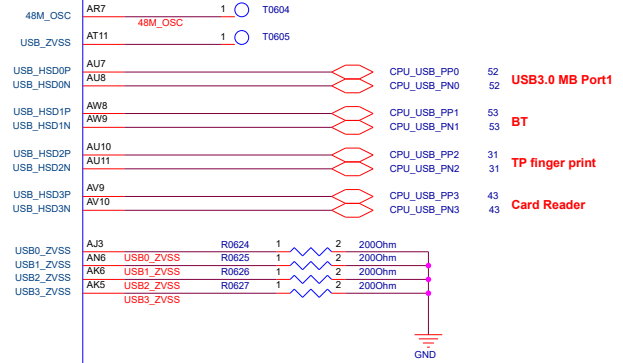


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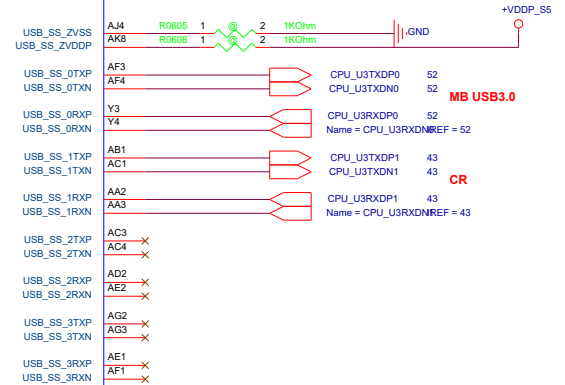


U0301E

SOCKET1331



teknisi-indonesia





Project Name

GL702ZM

Rev

R3.0

Title :

PW_+12VS_FAN

Size

B

Dept.:

NB Power team

Engineer:

Joe

Date: **Thursday, June 15, 2017**


Sheet

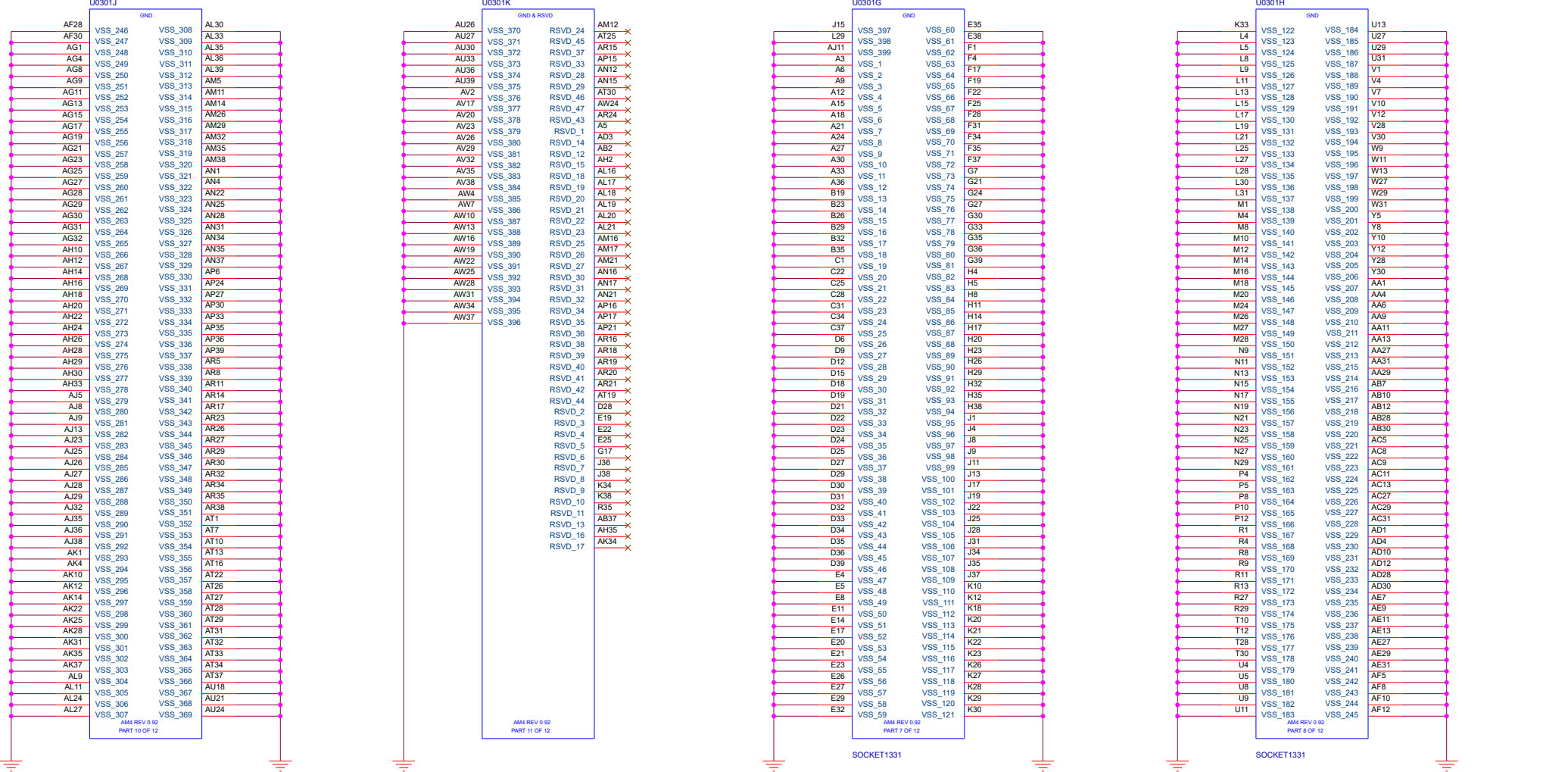
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of

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<Variant Name>

		Project Name		Rev
		GR702		2.0
Title : +VDDIO_AUDIO				
Size Custom	Dept.: ASUSTeK COMPUTER INC. Engineer: Joe			
Date: Thursday, June 15, 2017			Sheet	84 of 105




SOCKET1331

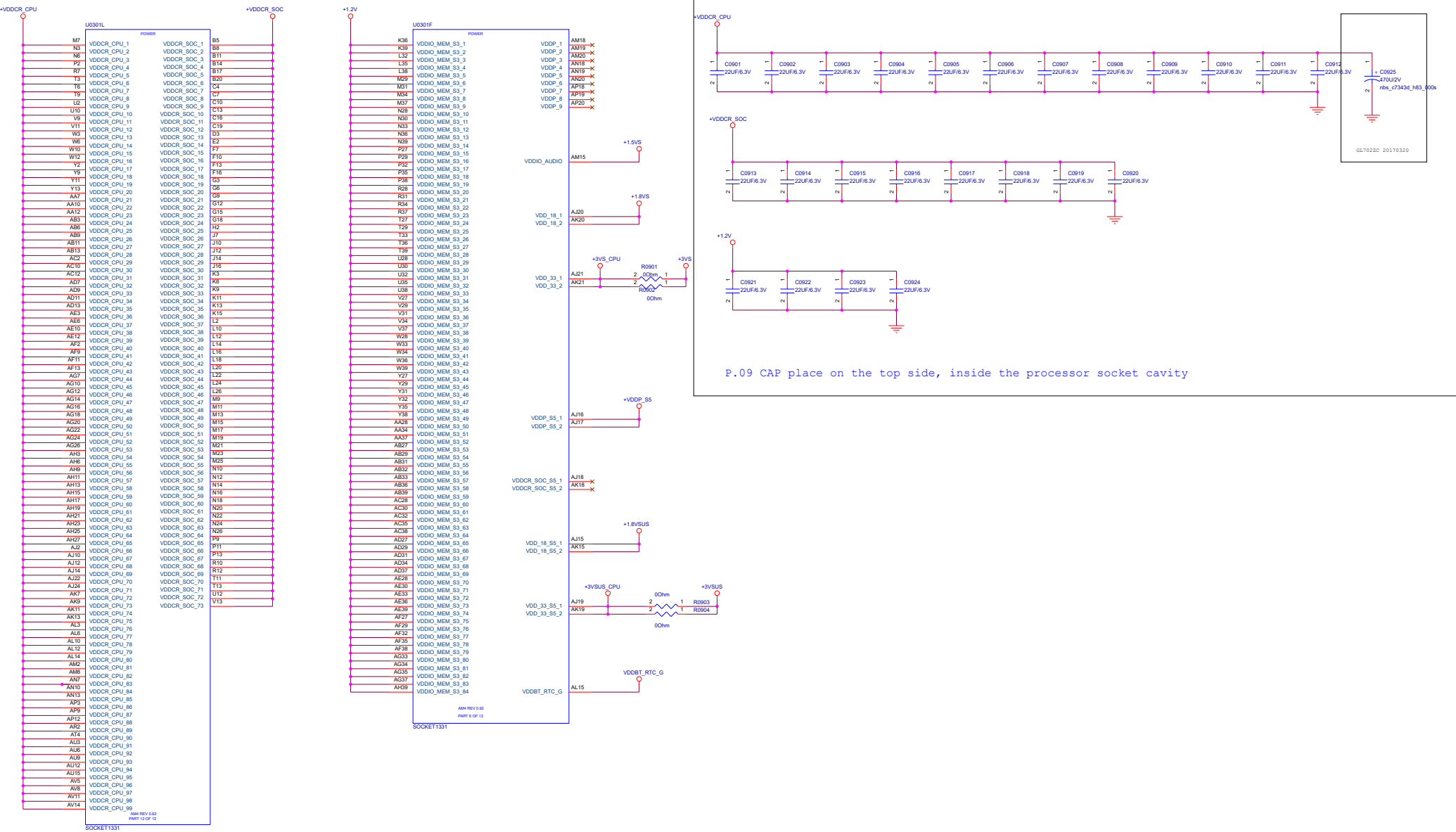
SOCKET1331

SOCKET1331

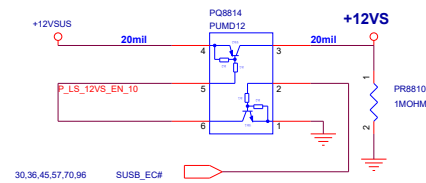
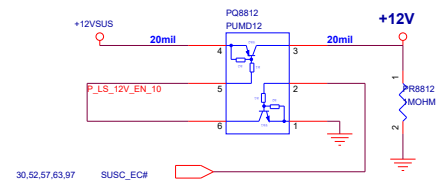
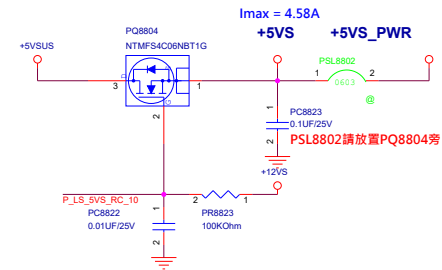
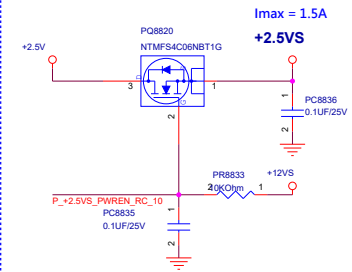
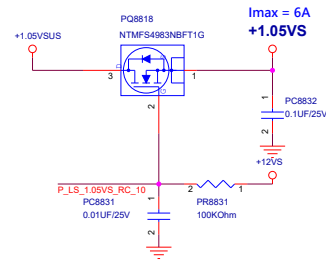
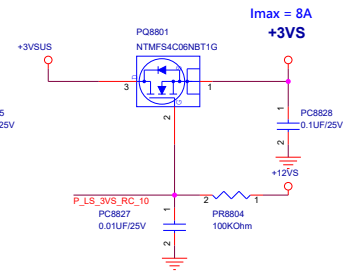
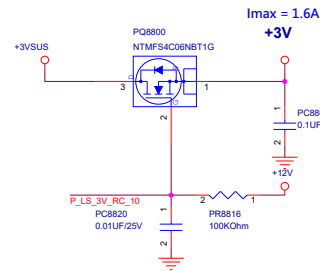
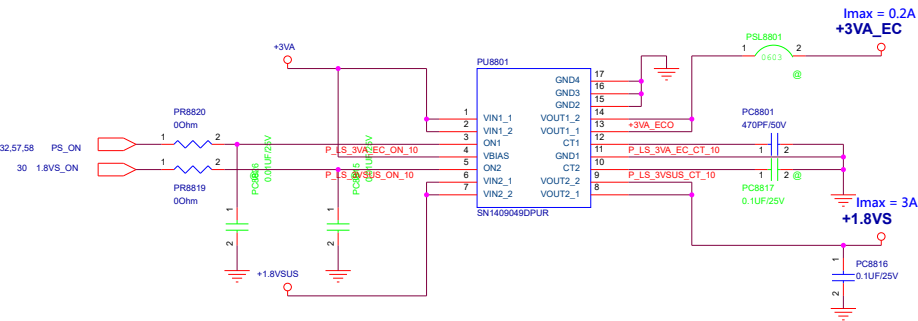
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		Project Name		Rev
		GR702		2.0
Title : +VDDIO_MEM_S3				
Size Custom	Dept.: ASUSTeK COMPUTER INC. Engineer: Joe			
Date: Thursday, June 15, 2017			Sheet 82	of 105



Load Switch

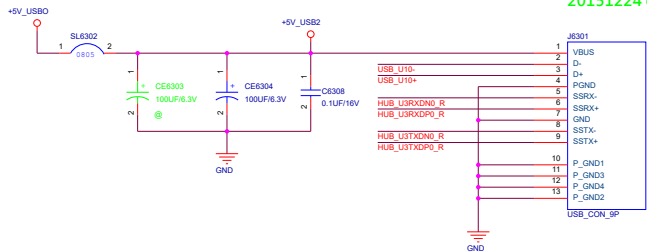
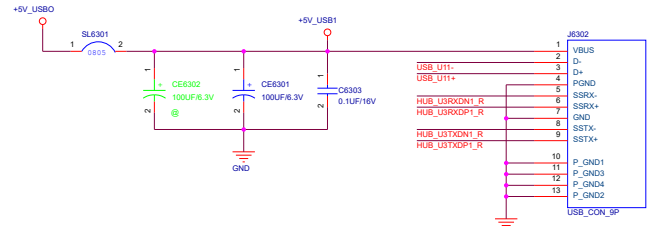
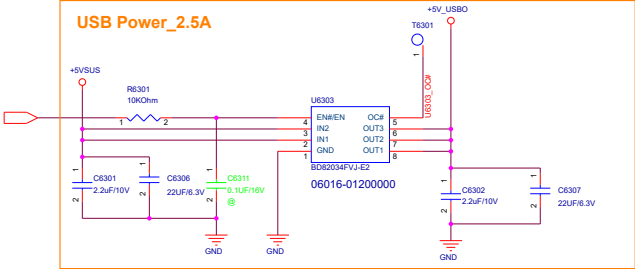
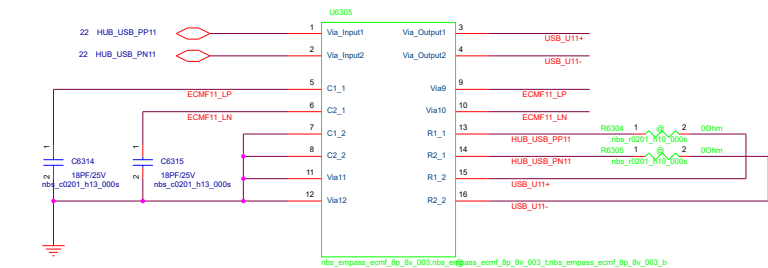
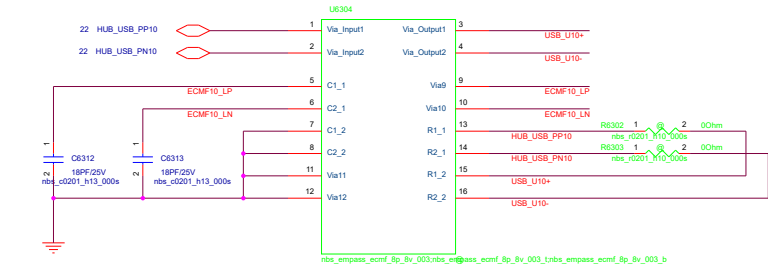


USB3.0
EMI-Protection

12/10/25
L5201, L5202, L5207, L5208
09G092090400

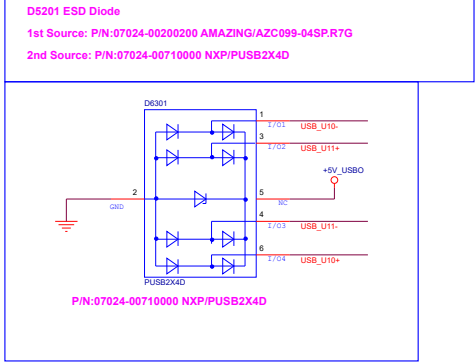


From PCH

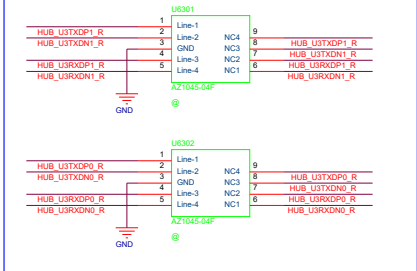


USB3.0/USB 2.0
ESD-Protection

R1.1-4/13-5



R1.1-4/13-5



U5201 & U5203 ESD PROTECTION
1st Source: P/N:07G028076030 ESD PROTECTION AZ1045-04F
2nd Source: P/N:07G028153010 ESD PROTECTION IP4284CZ10-TB

<Variant Name>

<Variant Name>



Project Name

GL702ZM

Rev

R1.0

Title : <Title>

Size

C

Dept.:

ASUSTeK COMPUTER INC. NB1

Engineer:

EE

Date: Thursday, June 15, 2017

Sheet

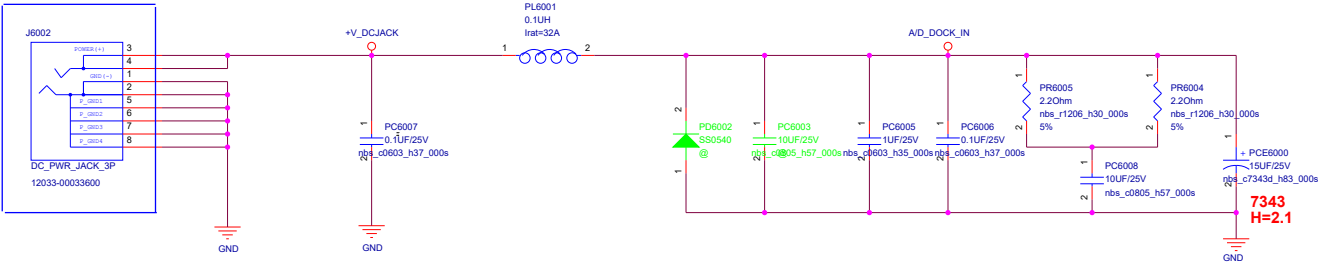
62

of

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DC-IN Connector

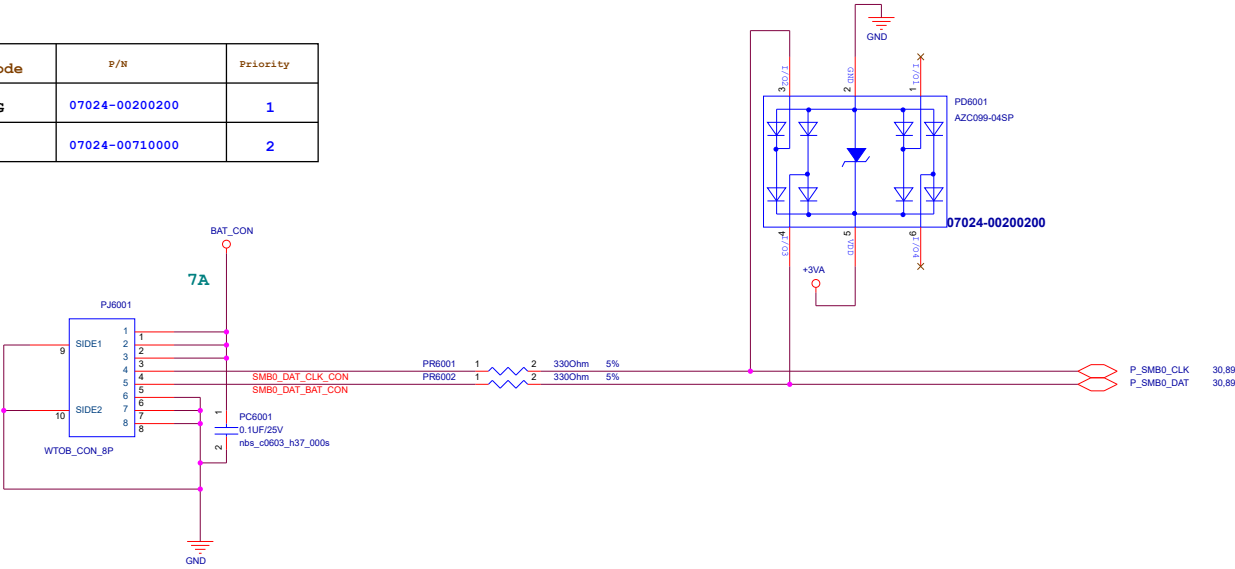
20170411 EE要求更換



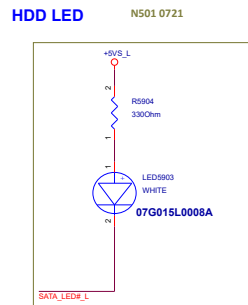
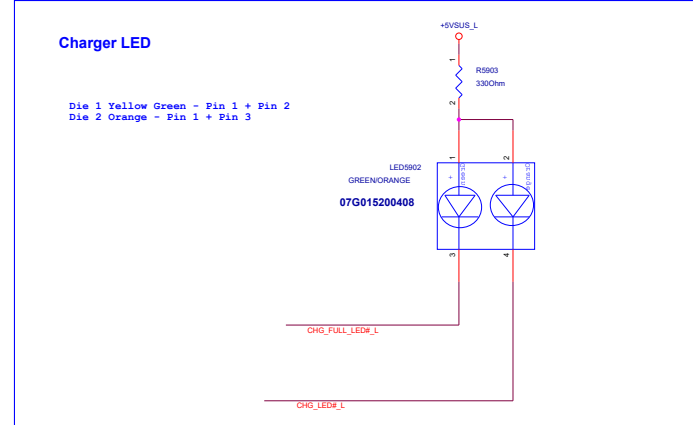
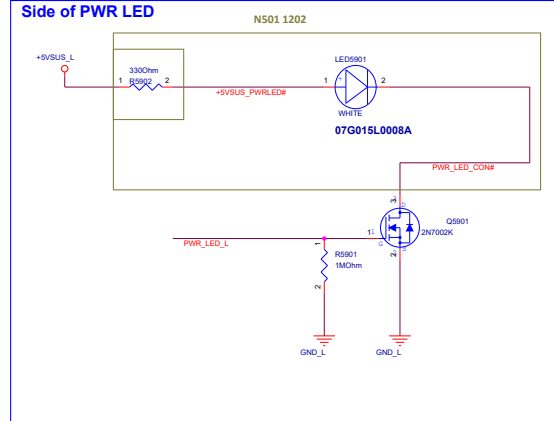
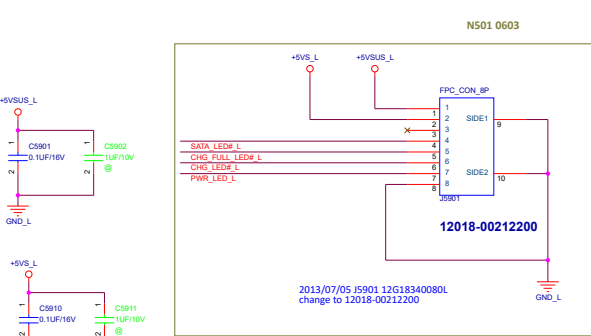
瓦數	P/N (With Cable)	P/N (W/O Cable)	Bead 數量
120W	14026-00040000	12033-00031000	5
180W	14026-00040000	12033-00031000	7
230W	TBD	12033-00030400	8
330W	TBD	12033-00050100	09G02X102300

Battery Connector

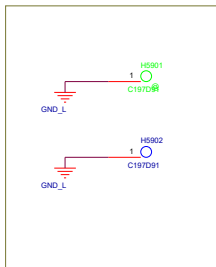
ESD Diode	P/N	Priority
AMAZING	07024-00200200	1
NXP	07024-00710000	2



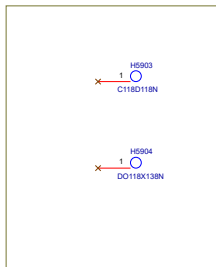
Note: Battery Connector 正確性與BAT1_IN_OC#是否預留!



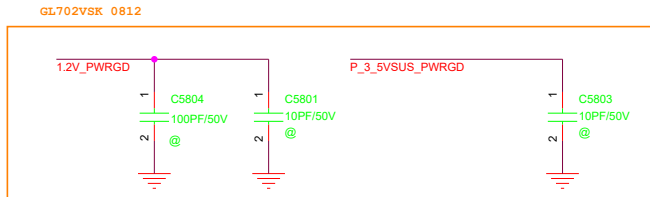
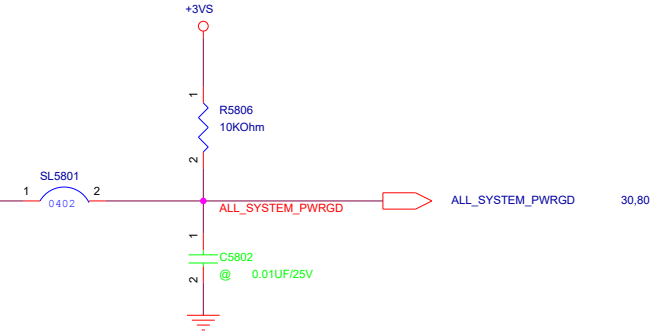
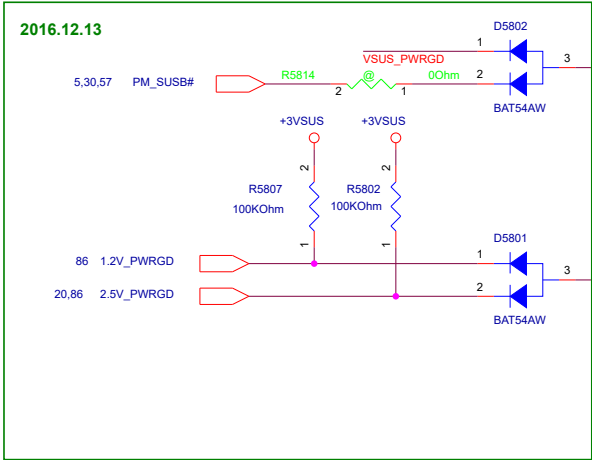
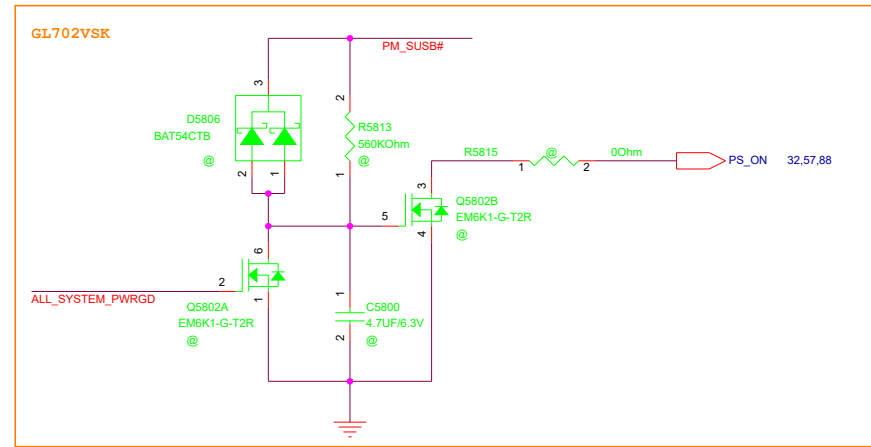
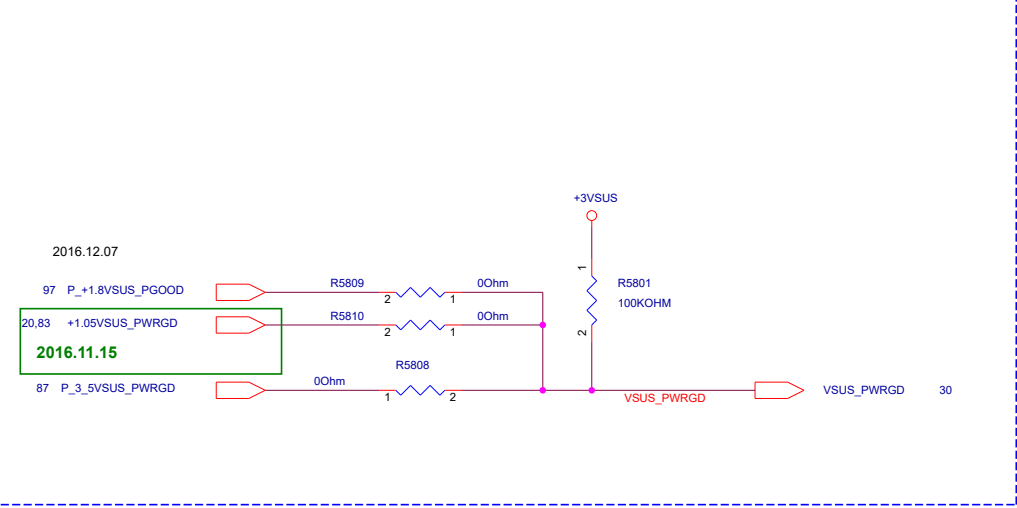
PTH screw hole



NPTH screw hole

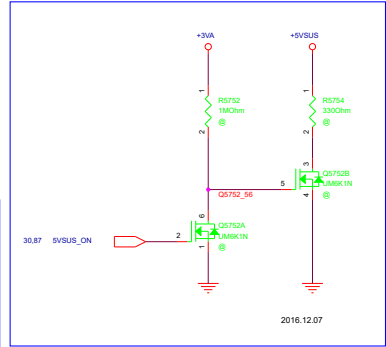
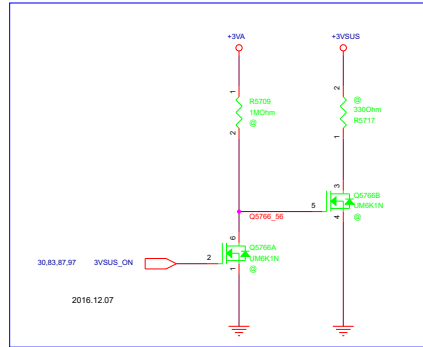
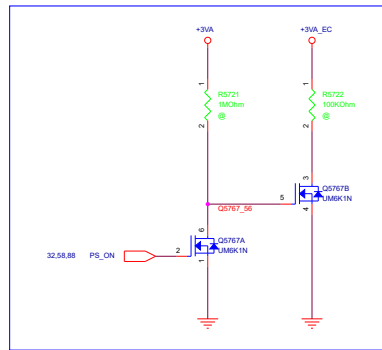
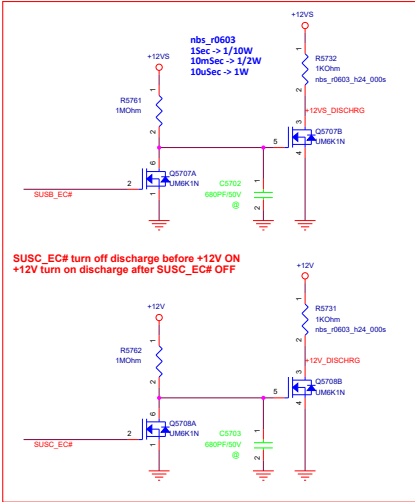
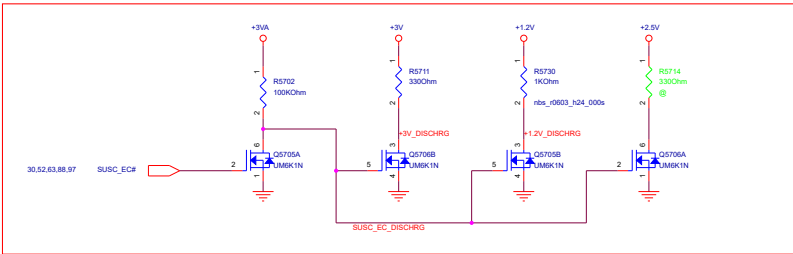
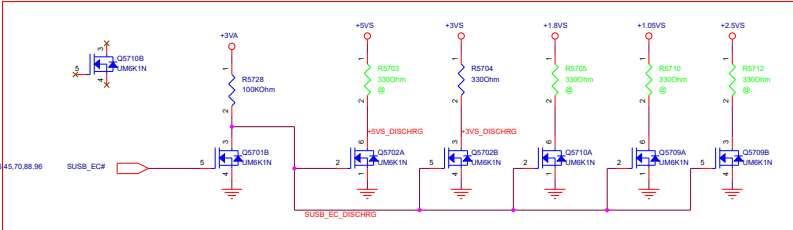


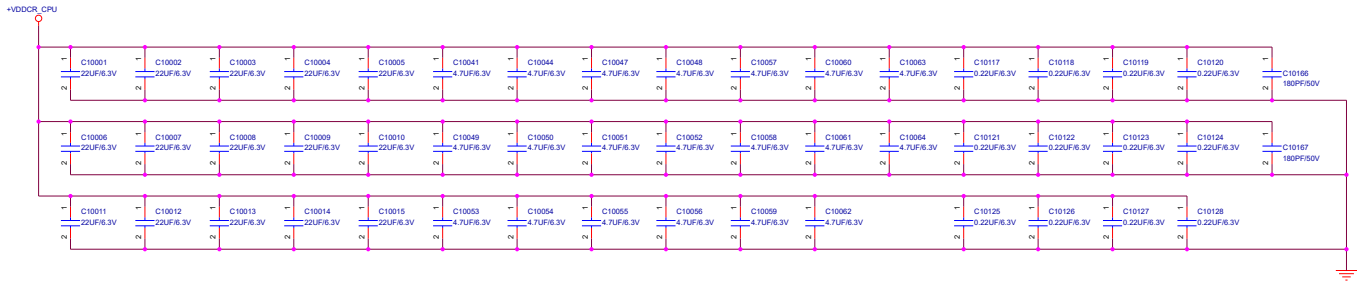
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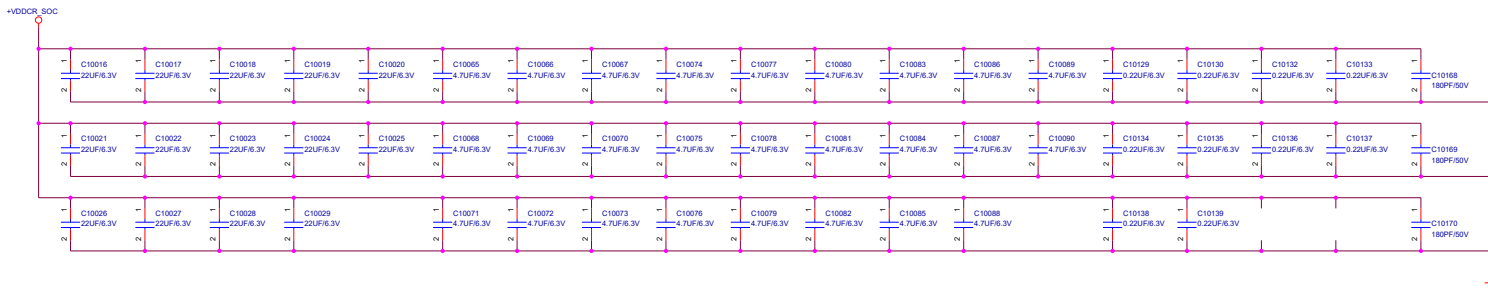
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ASUS		Project Name	Rev
GL702ZM			R1.0
Title : Power Protect			
Size	Dept.:	ASUSTeK COMPUTER INC.	Engineer: EE
Custom			
Date: Thursday, June 15, 2017	Sheet	58	of 102

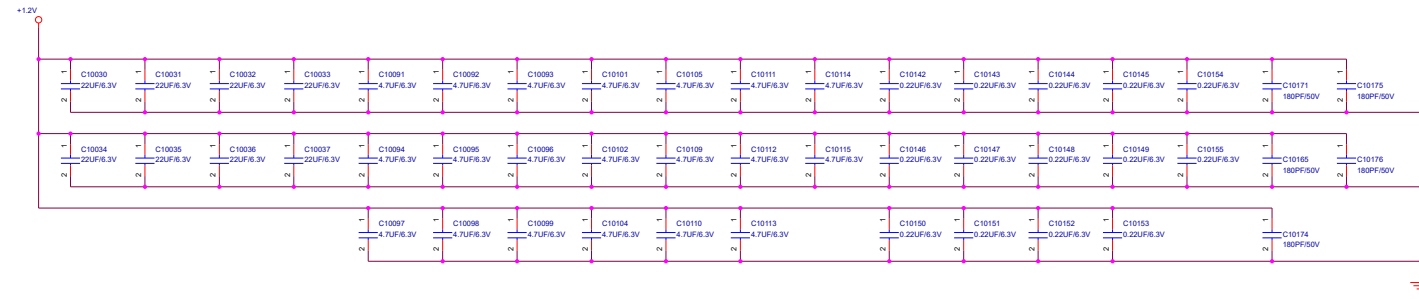




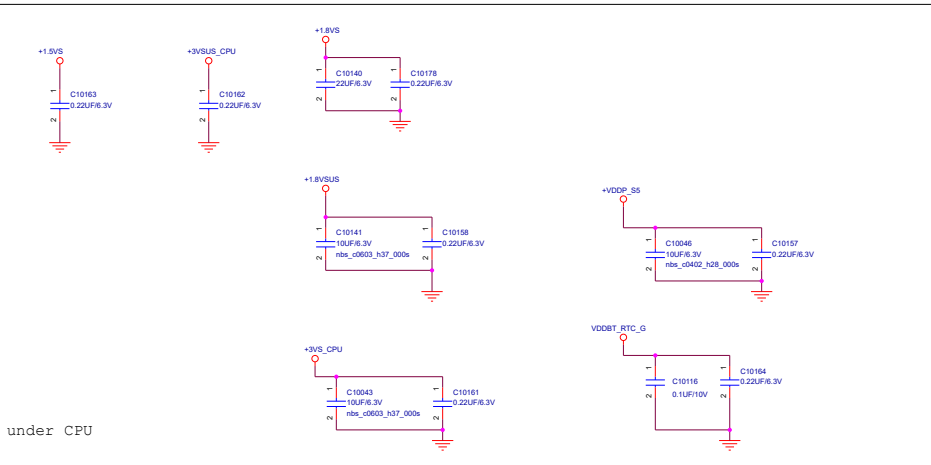
under CPU,
 $22\mu F * 15$
 $4.7\mu F * 20$
 $0.22\mu F * 12$
 $180pF * 2$

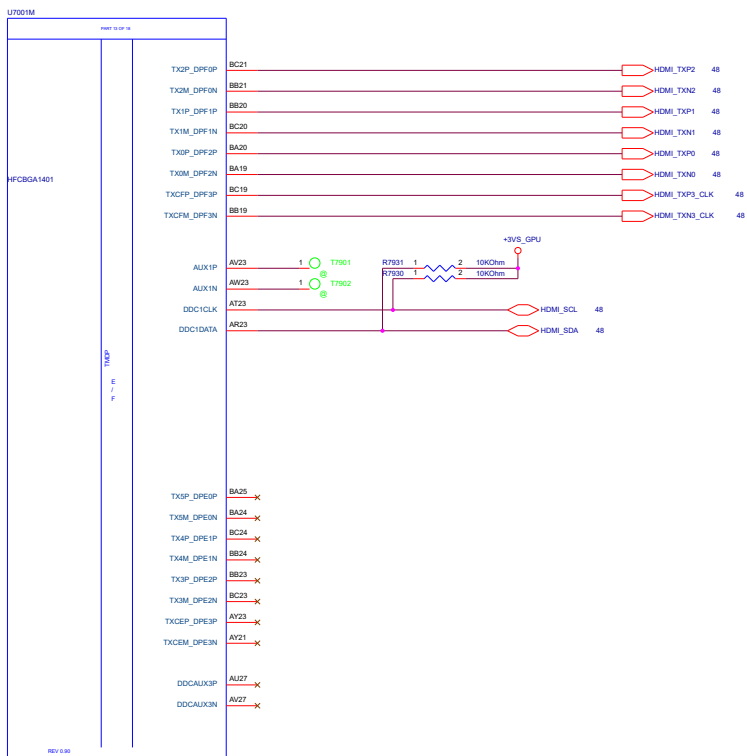
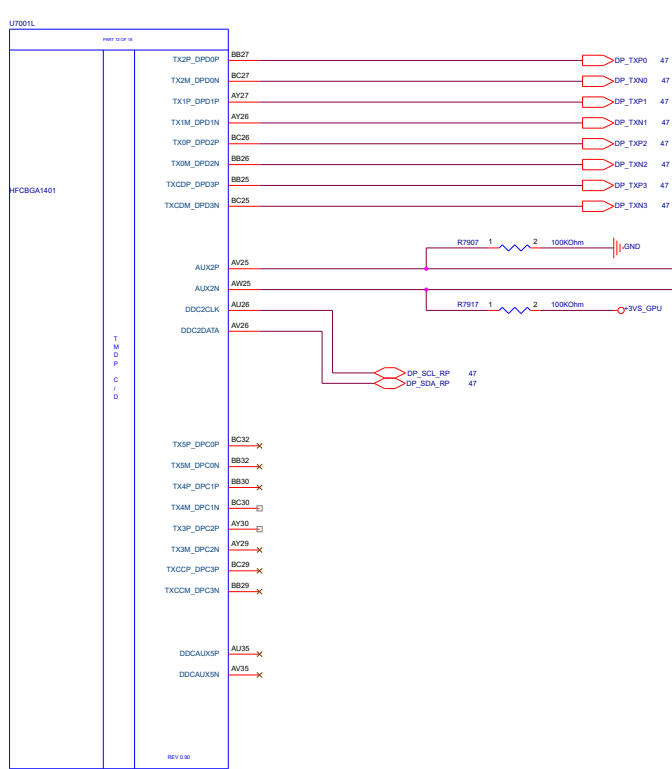
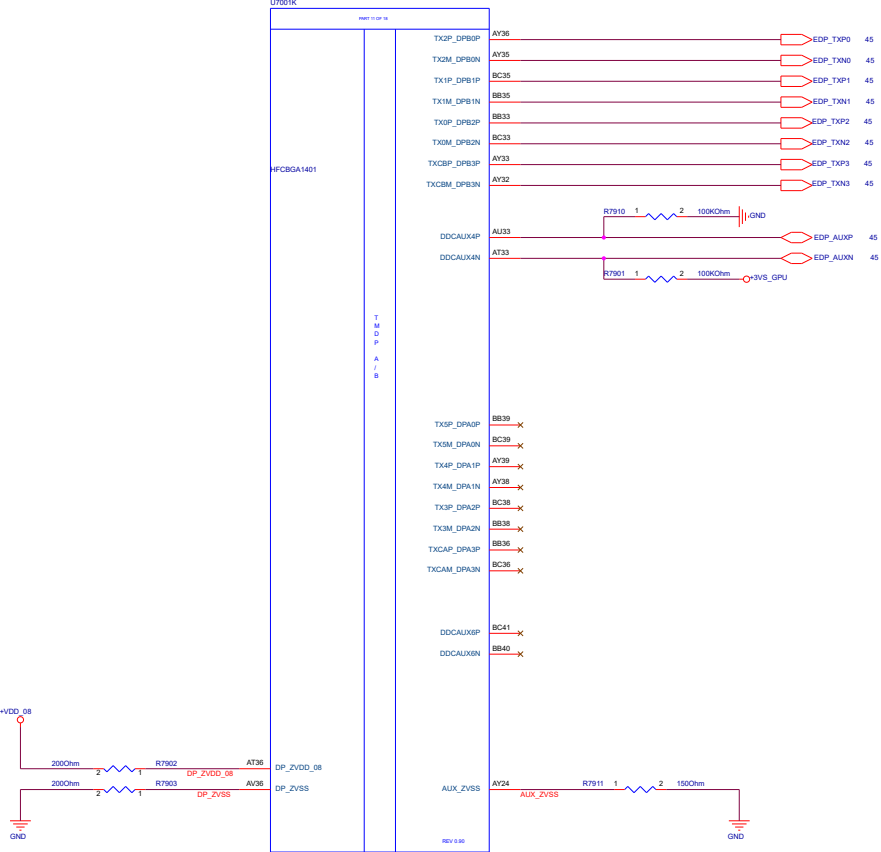


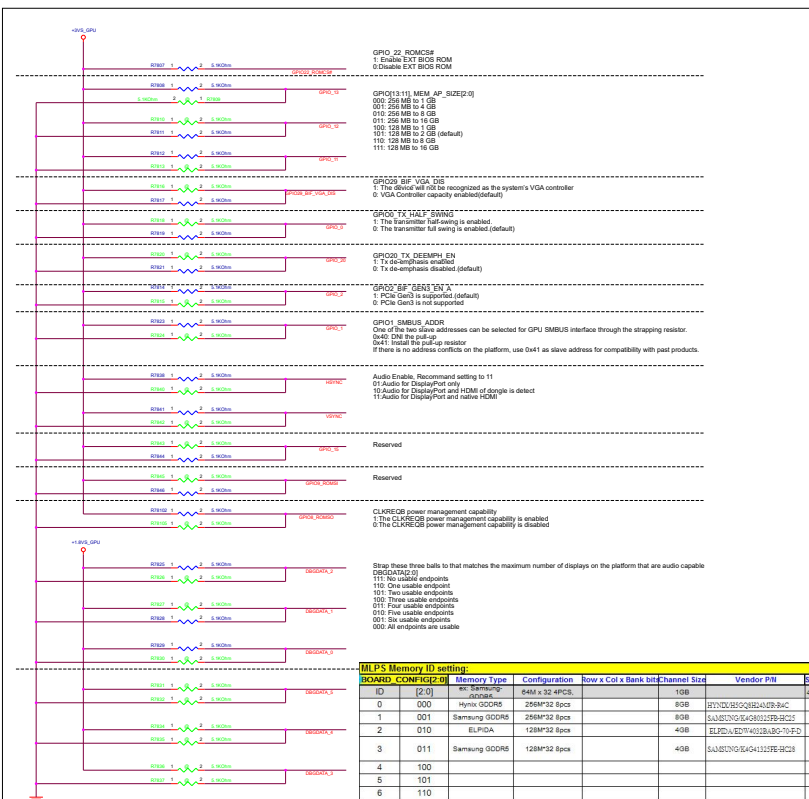
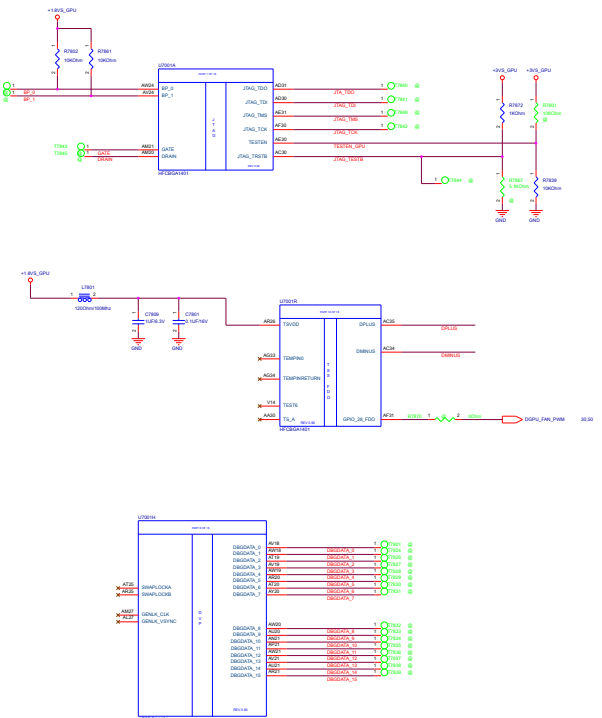
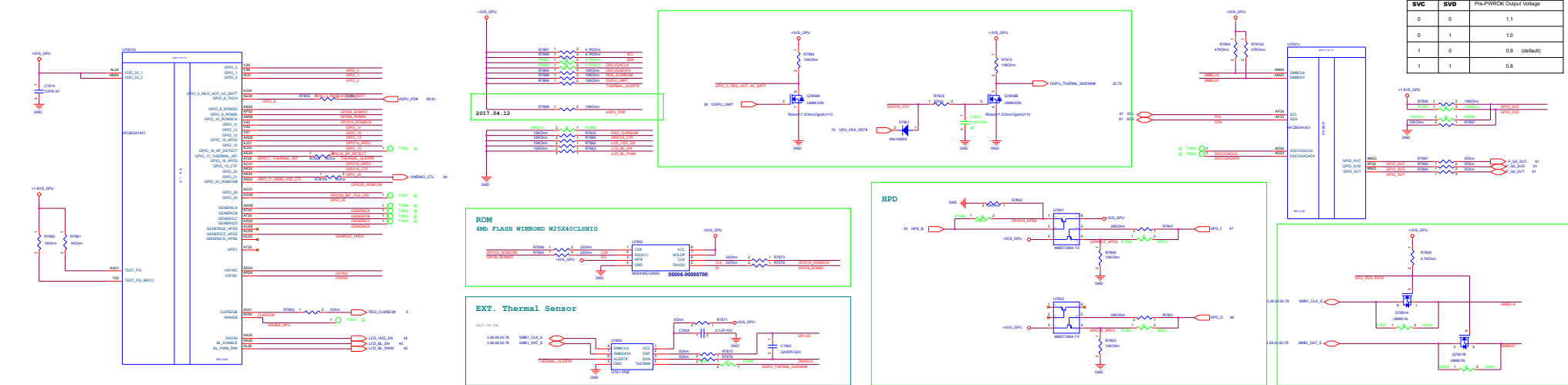
under CPU,
 $22\mu F * 14$
 $4.7\mu F * 26$
 $0.22\mu F * 10$
 $180pF * 3$



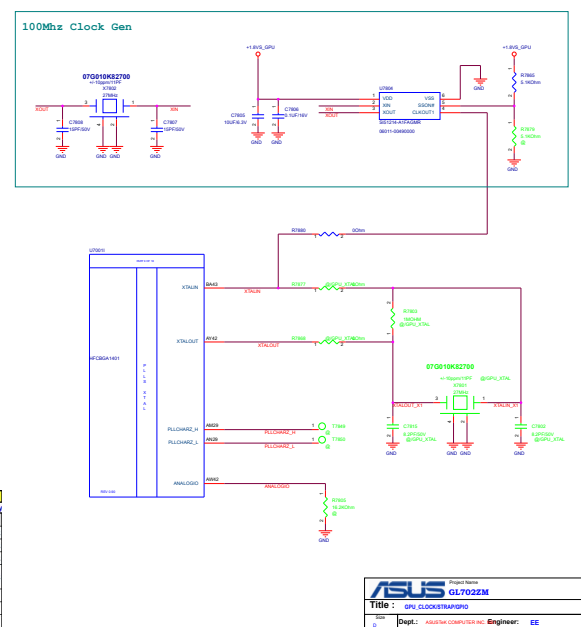
under CPU,
 $22\mu F * 8$
 $4.7\mu F * 20$
 $0.22\mu F * 14$
 $180pF * 4$

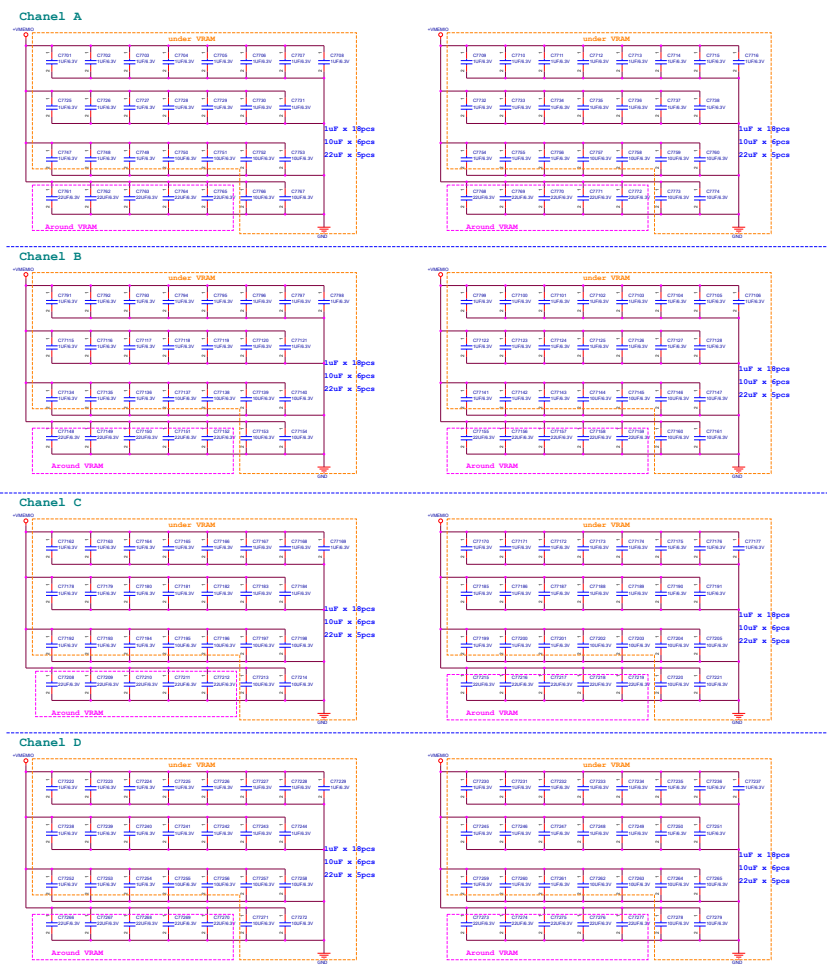




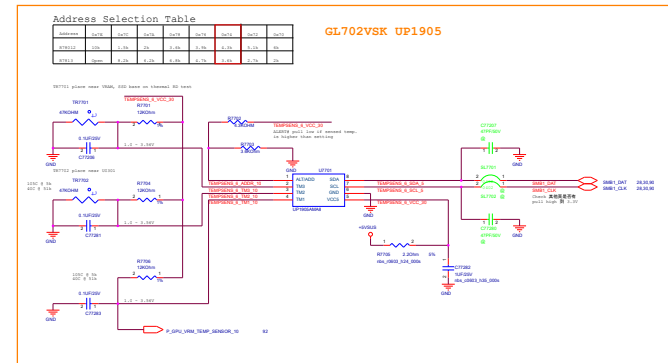
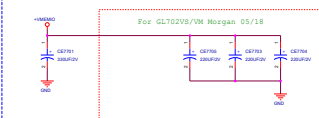
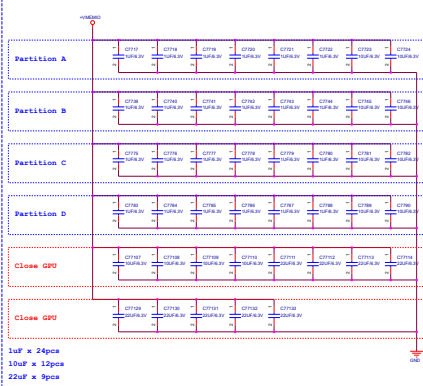


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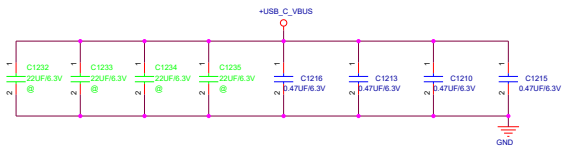
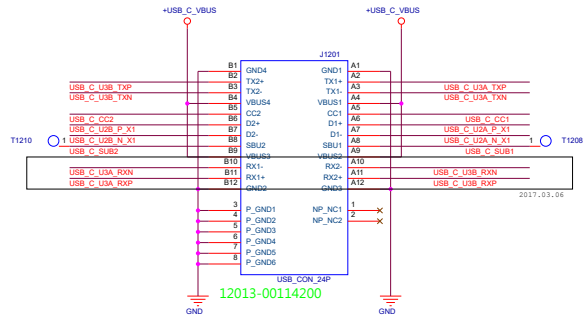
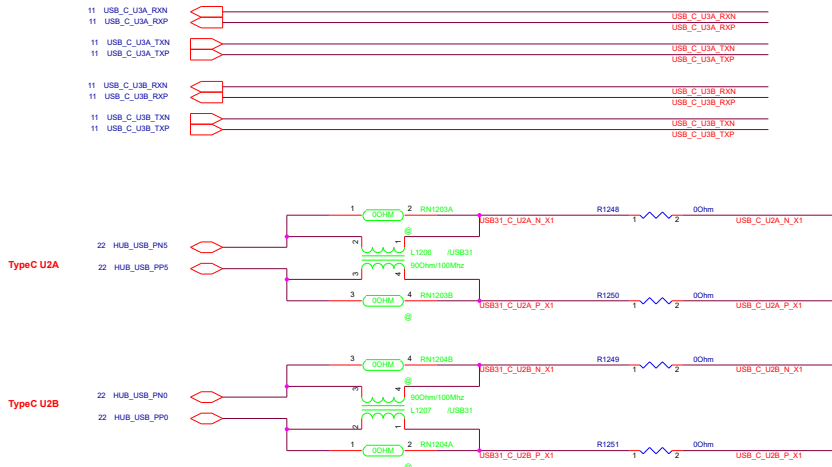




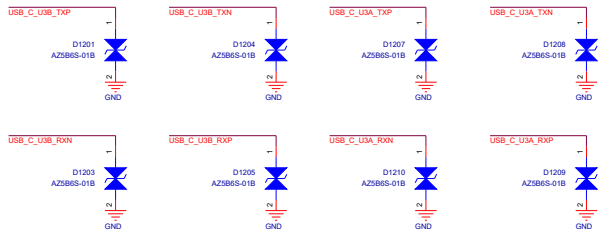
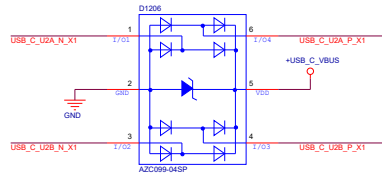
VRAM FWR_FBVDQ



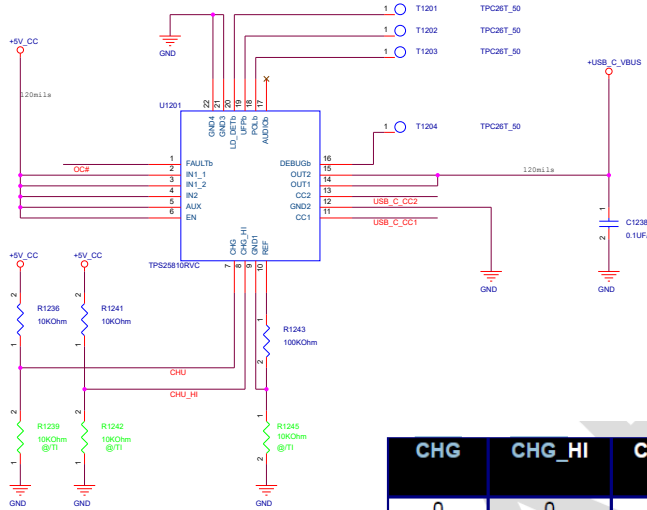
USB type C



ESD-Protection



Set CC
I limit = 3A



CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A



Project Name

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Title : <Title>

Size


Custom

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<Variant Name>

		Project Name GL702ZM		Rev R1.0
Title : <Title>				
Size A	Dept.: ASUSTeK COMPUTER INC. NB1 Engineer: EE			
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<Variant Name>



Project Name

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Rev

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Title :

Size

Custom

Dept.:

ASUSTeK COMPUTER INC. NB1

Engineer:

EE

Date: Thursday, June 15, 2017


Sheet

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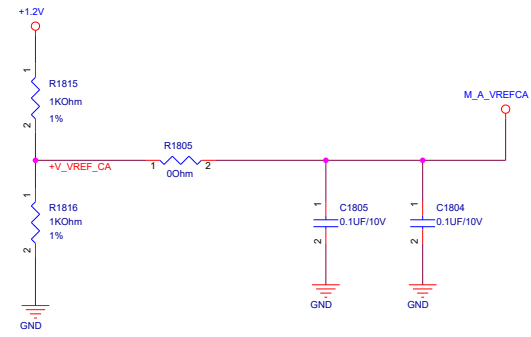
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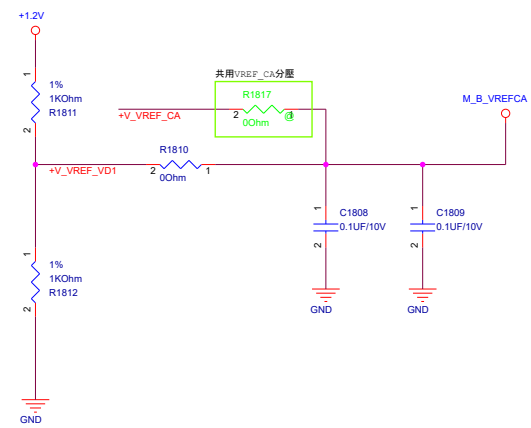
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Title :				
Size Custom	Dept.: ASUSTeK COMPUTER INC. NB1 Engineer: EE			
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SO-DIMM0 Vref

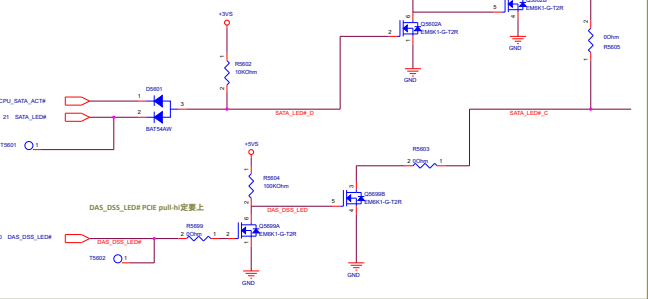


SO-DIMM1 Vref



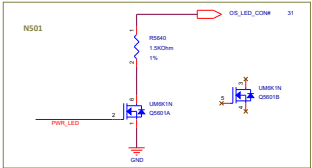
2017.04.12 modify

HDD LED & PCIE SSD LED

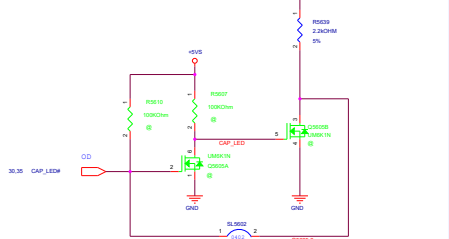


R10_09 Samsung LED Issue

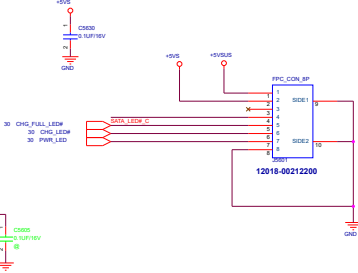
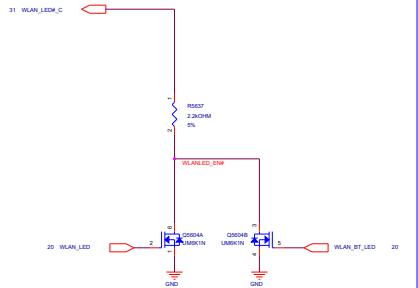
OS LED



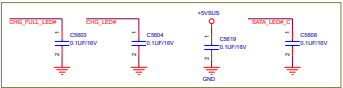
CAP LED



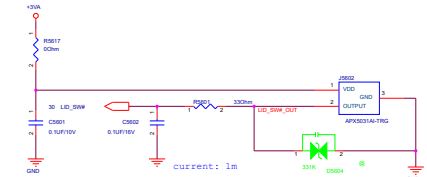
WireLess LED



NS01 0729 EMI



HALL SENSOR 20160218
06033-00140000



<Variant Name>



Project Name

GL702ZM

Rev

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Title : <Title>

Size

C

Dept.:

ASUSTeK COMPUTER INC. NB1

Engineer:

EE

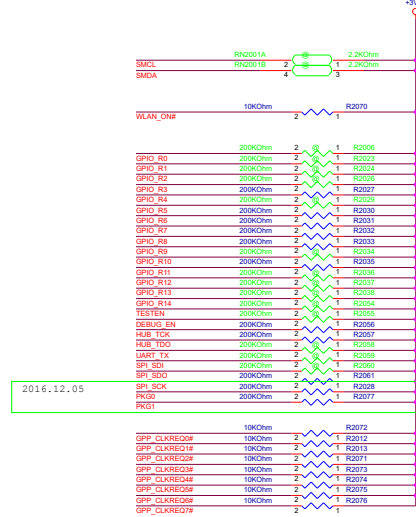
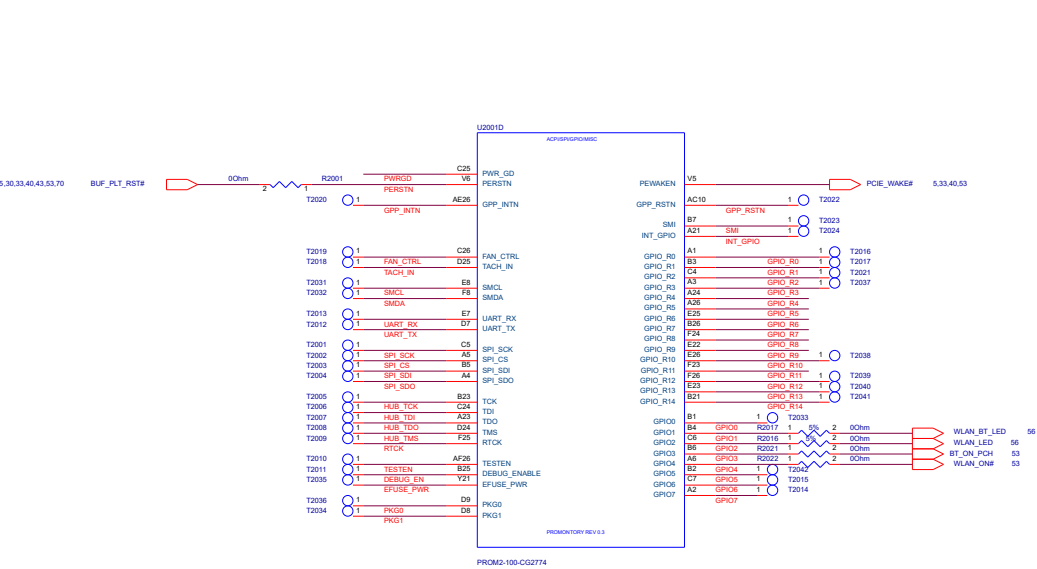
Date: Thursday, June 15, 2017

Sheet

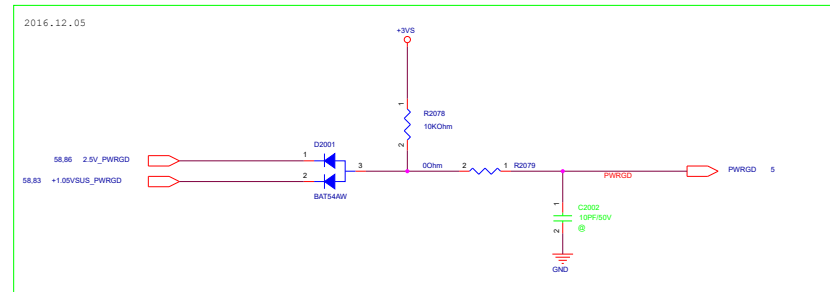
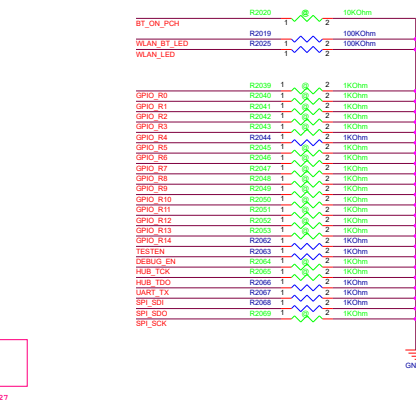
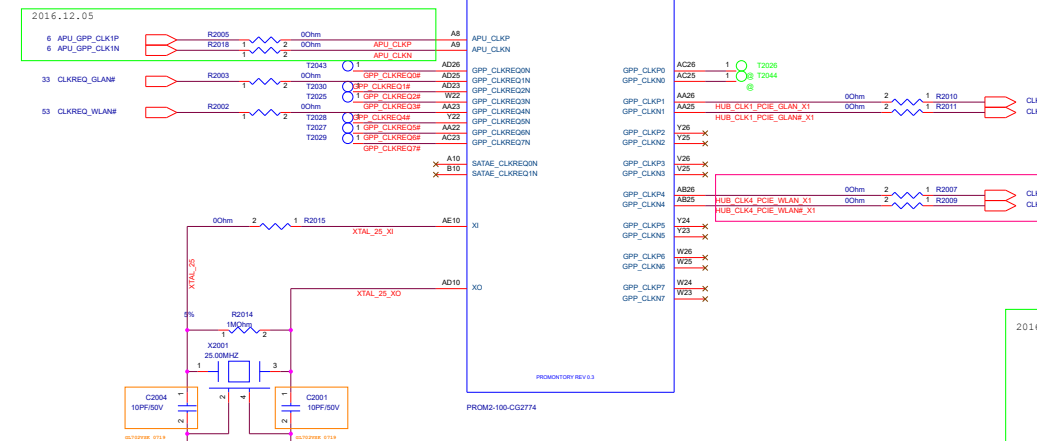
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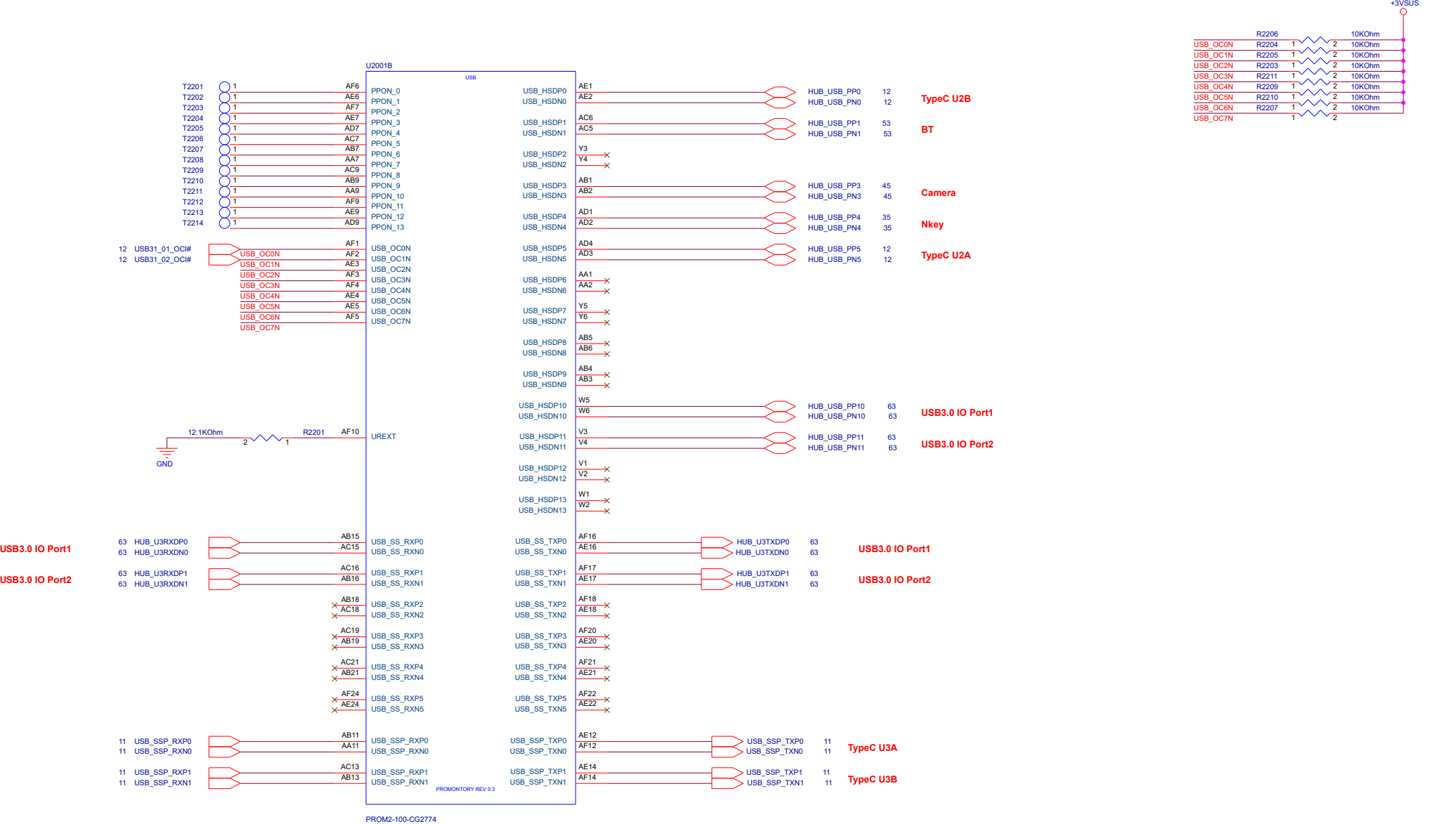
of

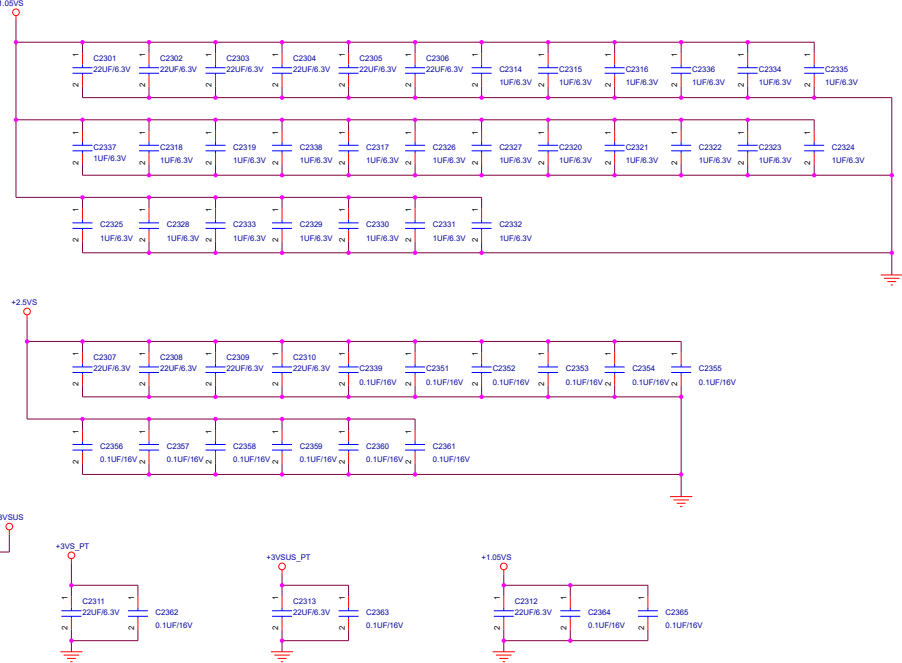
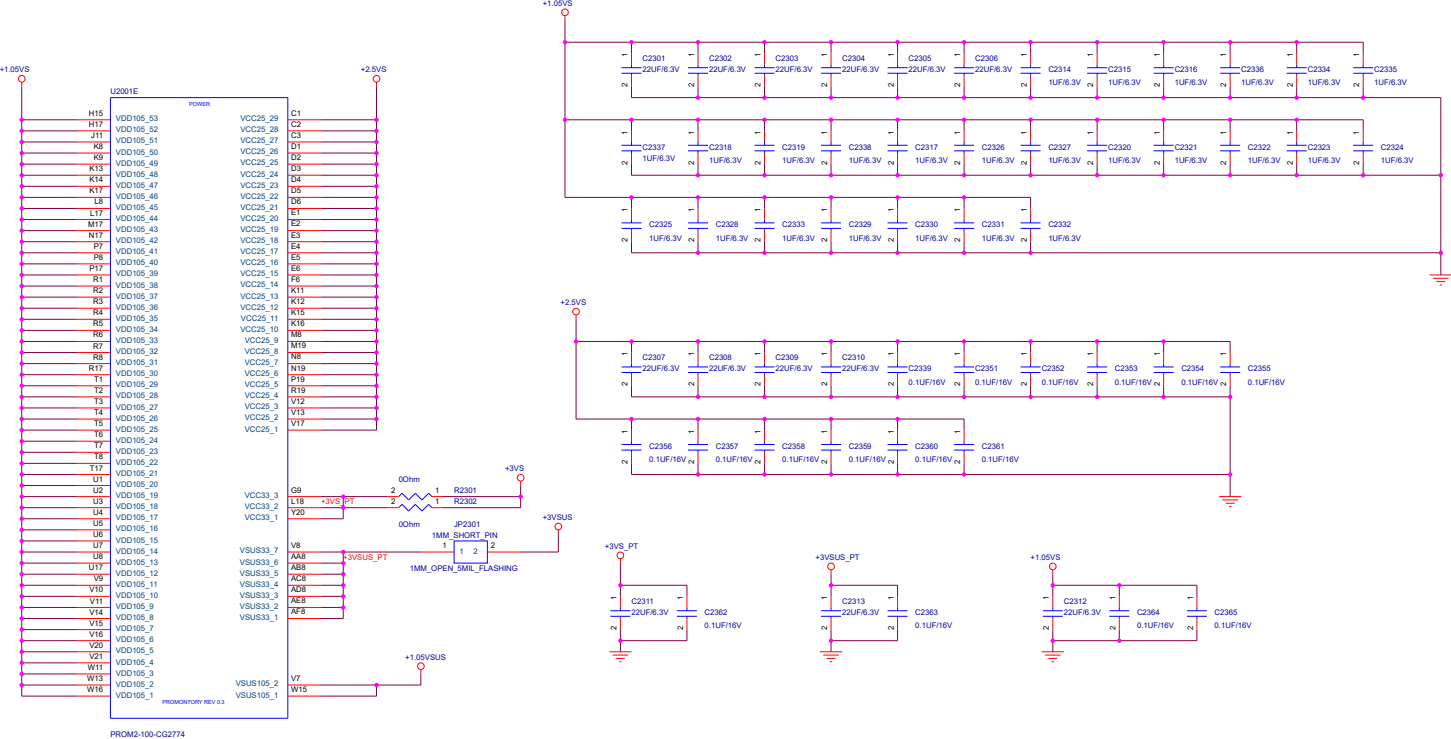
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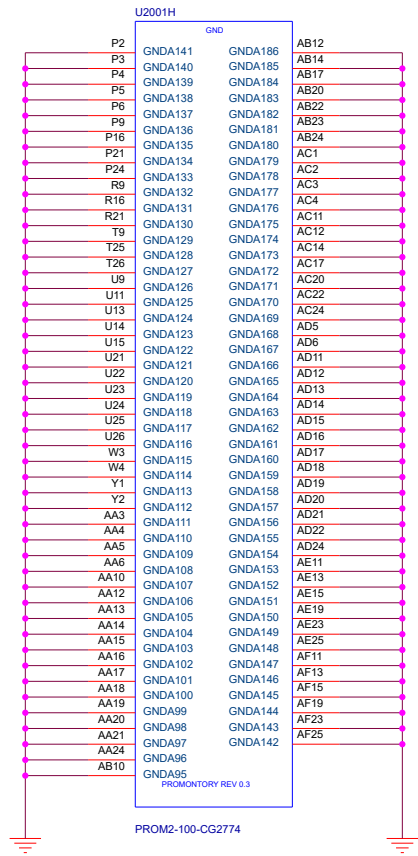
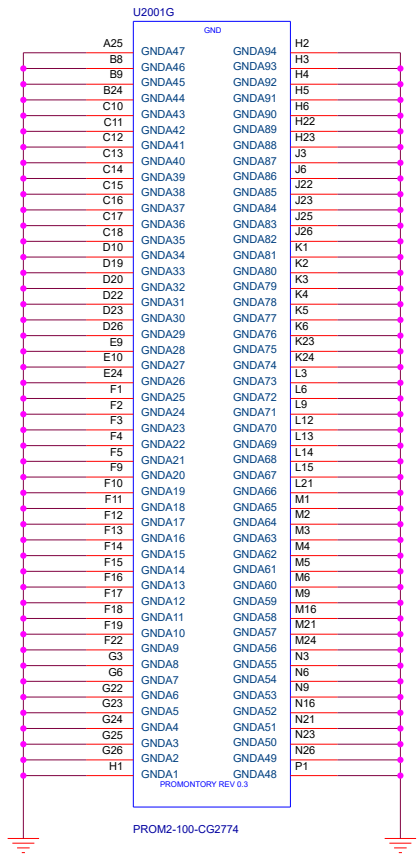
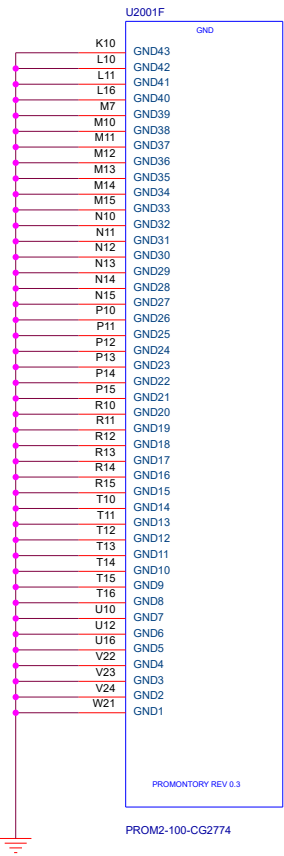
Strapping Pins	FUNCTION
TESTEN	TEST mode enable High:Test mode Low:Function mode
IFDET1	SATA Express port1 High:PCIe mode Low:SATA mode
IFDET0	SATA Express port0 High:PCIe mode Low:SATA mode
DEBUG_ENABLE	High:Debug mode Low:Function mode
TCK(DEBUG_SEL1) TDO(DEBUG_SEL0)	11: Debug signal group3 output 10: Debug signal group2 output 01: Debug signal group1 output 00: Debug signal group0 output
UART_TX (GPP_GL_SET1)	GPP Group1 11: 1 PCIe*4 10: 1 PCIe*2 + 2 PCIe*1 01: 4 PCIe*1 00: Reserved
SPI_SDI (GPP_GL_SET0)	GPP Group0 11: 1 PCIe*4 10: 1 PCIe*2 + 2 PCIe*1 01: 4 PCIe*1 00: Reserved
SPI_SDO (GPP_G0_SET1)	GPP Group0 11: 1 PCIe*4 10: 1 PCIe*2 + 2 PCIe*1 01: 4 PCIe*1 00: Reserved
SPI_SCK (GPP_G0_SET0)	GPP Group0 11: 1 PCIe*4 10: 1 PCIe*2 + 2 PCIe*1 01: 4 PCIe*1 00: Reserved
GPIO_R4	High:GPP clock source from APU CLKP/N Low:GPP clock source from CrystaL
GPIO_R5	High:USBC SSC disable Low:USBC SSC enable
GPIO_R6	High:SATA SSC disable Low:SATA SSC enable
GPIO_R7	High:SATA Express SSC disable Low:SATA Express SSC enable
GPIO_R8	High:GPP SSC disable Low:GPP SSC enable
GPIO_R11	High:GPP clock output enable Low:GPP clock output disable







Main Board





Project Name

GL702ZM

Rev

R1.0

Title : <Title>

Size

A

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Engineer: **EE**

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Rev

R1.0

Title : **<Title>**

Size

B

Dept.:

ASUSTeK COMPUTER INC. NB1

Engineer:

EE

Date: **Thursday, June 15, 2017**

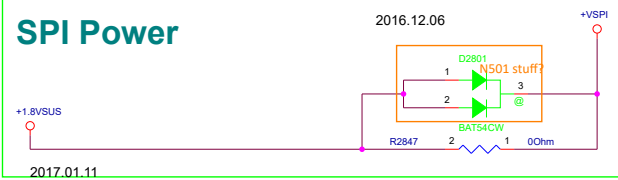
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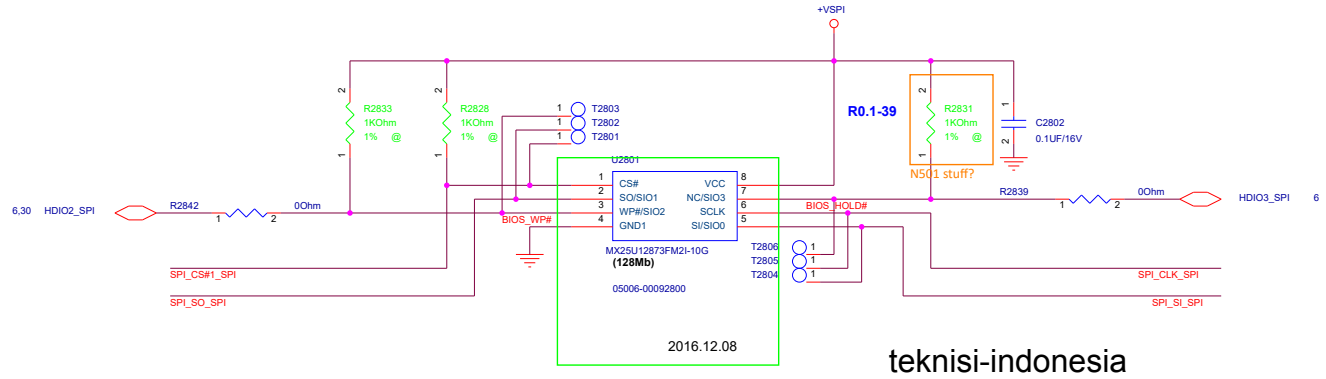
102

SPI Power



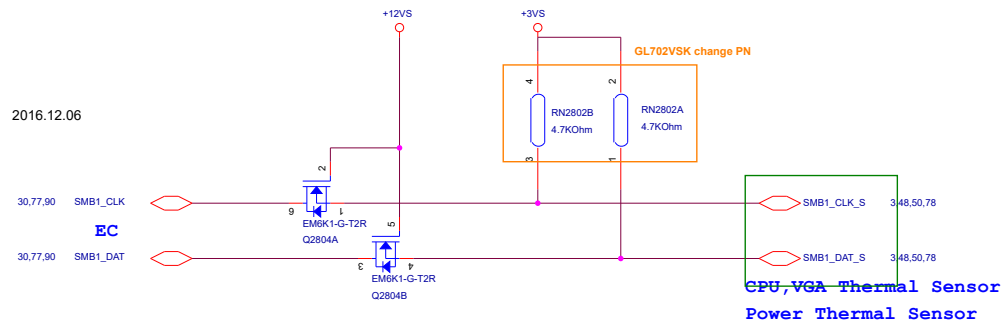
1st SPI ROM

Main: 05006-00010500 (fixed quad bit)

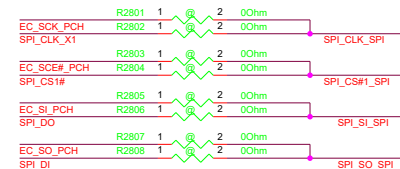
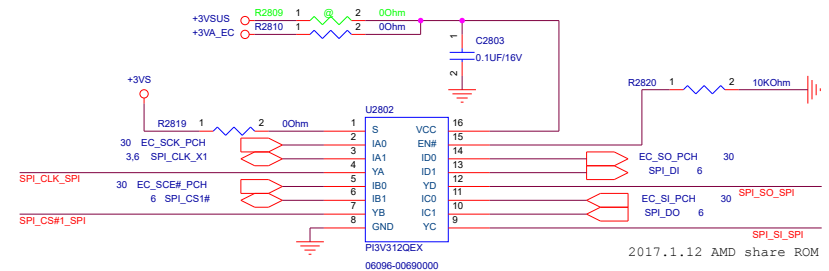
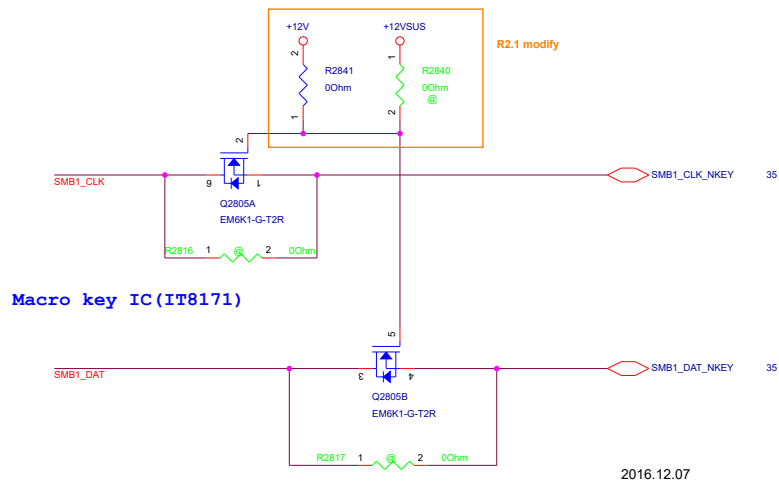
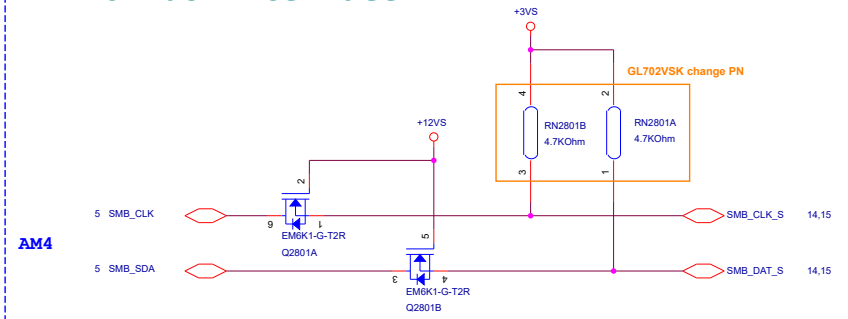


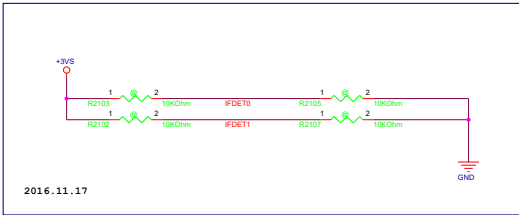
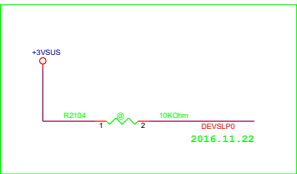
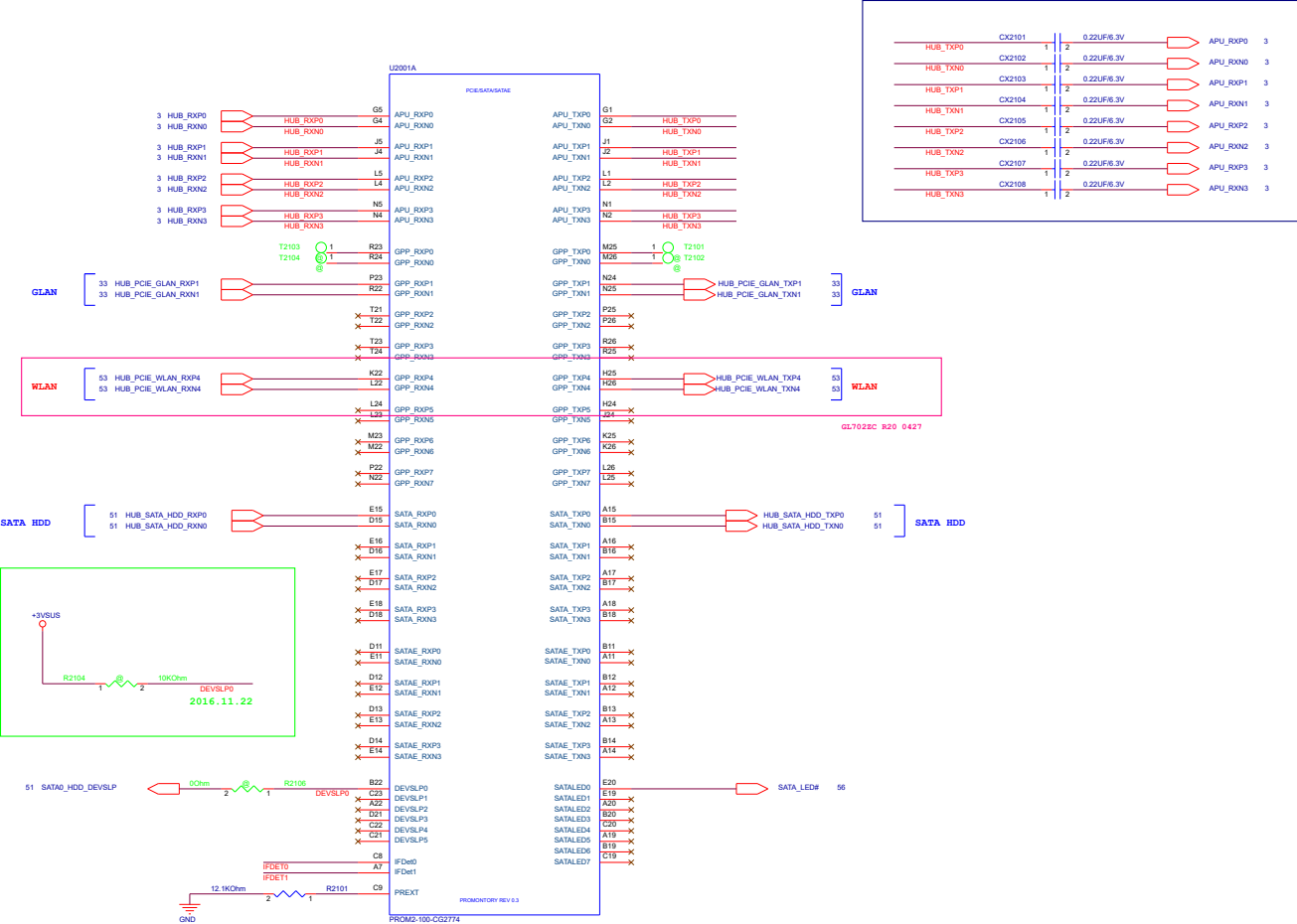
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System Management Interface

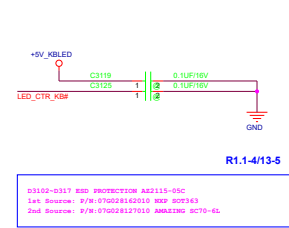
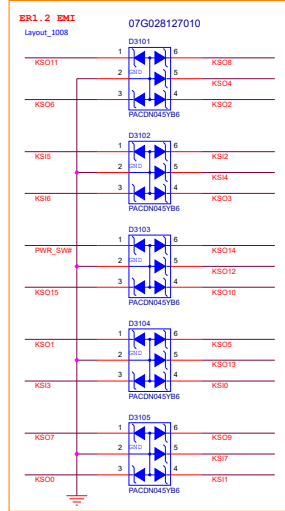
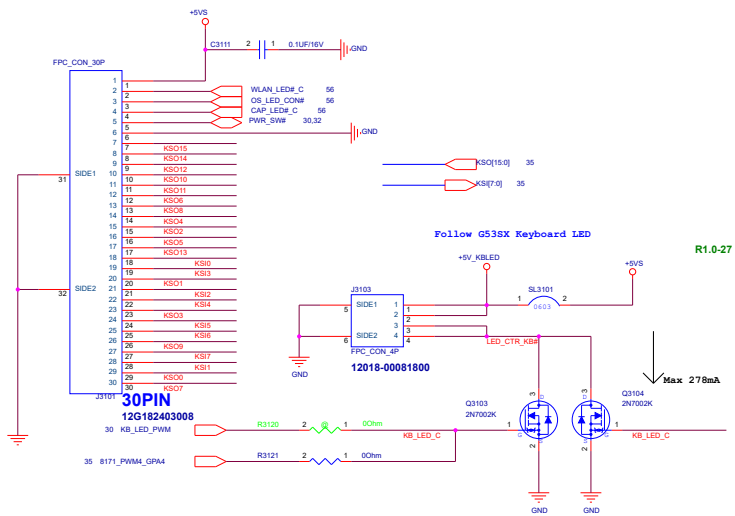


SMBus Interface

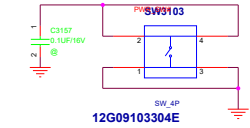




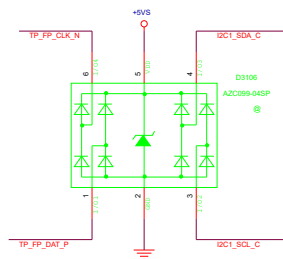
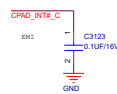
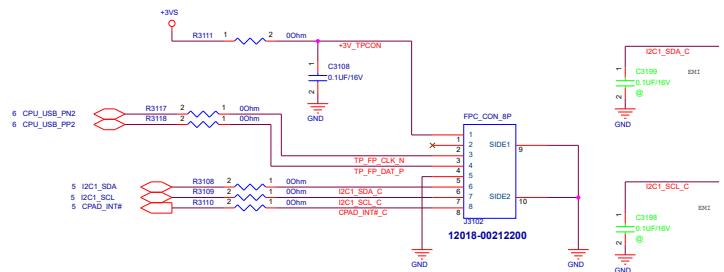
Keyboard Connector



POWER button for SR



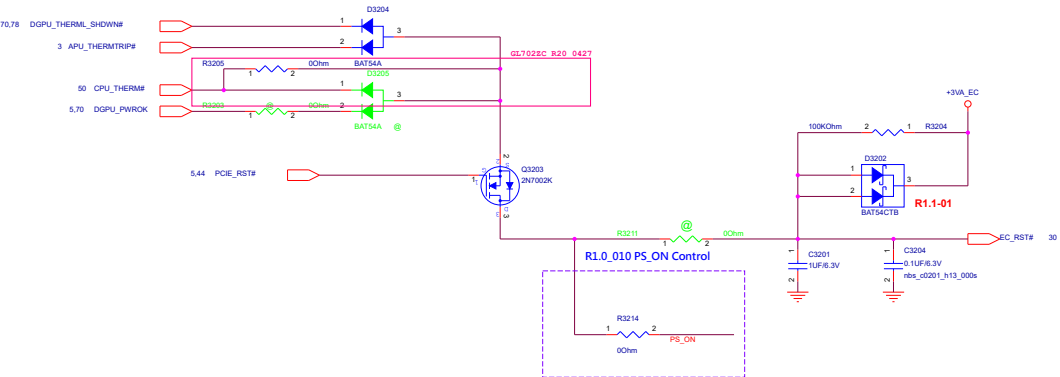
Click touch Pad Connector



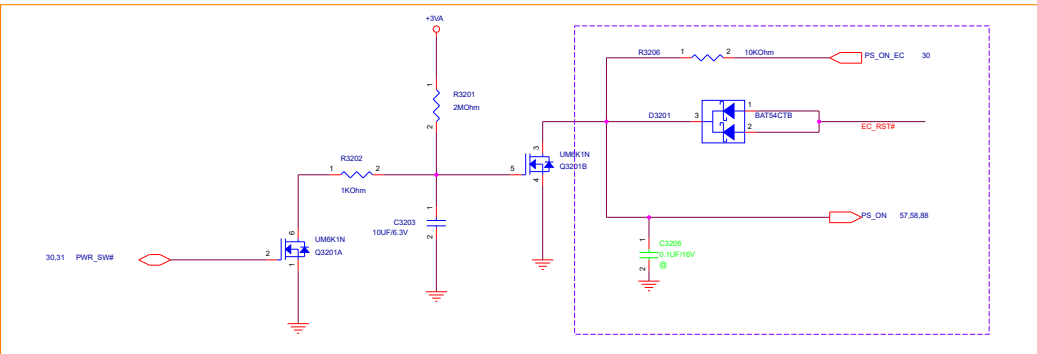
<<Variant Name>

Reset Circuit

Pull up +3VSG through R7507(10kOhm=>100kOhm)
 When +3VSG ready, R7507(10kOhm) and R5006(7.5kOhm) will be in parallel.
 The CPU temperature point is protected ahead of time.
 Increasing R7507 value can reduce to affect R5006.

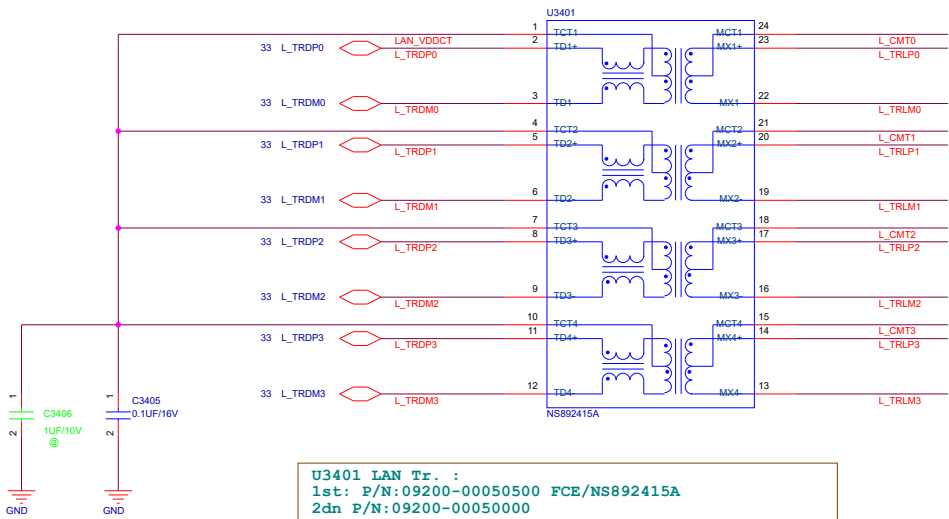


Battery embedded (press pwr_sw 10sec, then reset ec)

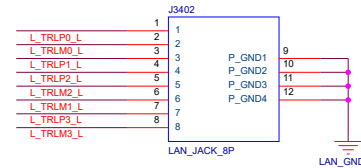


EC power off solution:
 Solution1 Mount R3206, D3201/ Unmount R3216
 Solution2 Mount R3206/R3216/ Unmount D3201- for reserved 0402 footprint

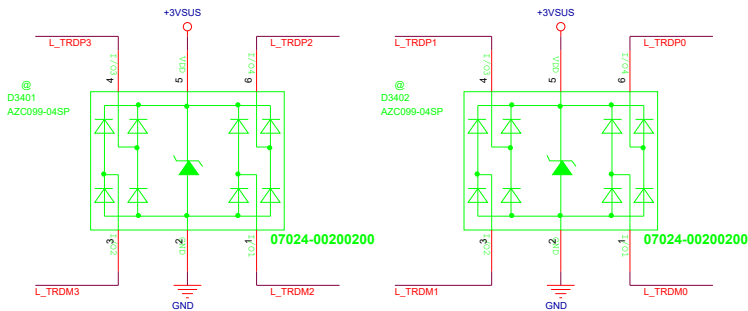
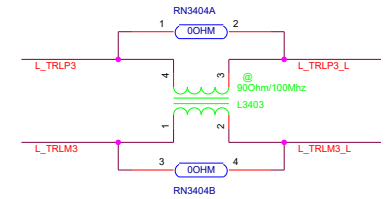
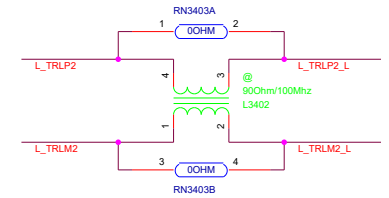
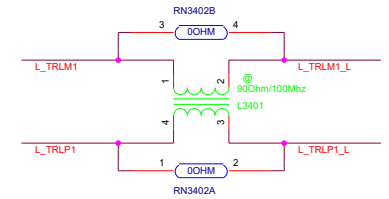
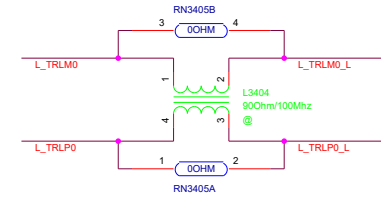
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ASUS		GL702ZM	R1.0
Title : RST_Reset Circuit			
Size	Dept.	ASUSTek COMPUTER INC.	Engineer: EE
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LAN Connector



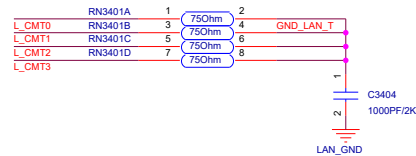
P/N:12014-00693100 SANTA/130470-17
20160108 check



D3401, D3402 ESD Diode

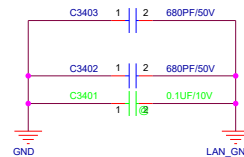
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2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

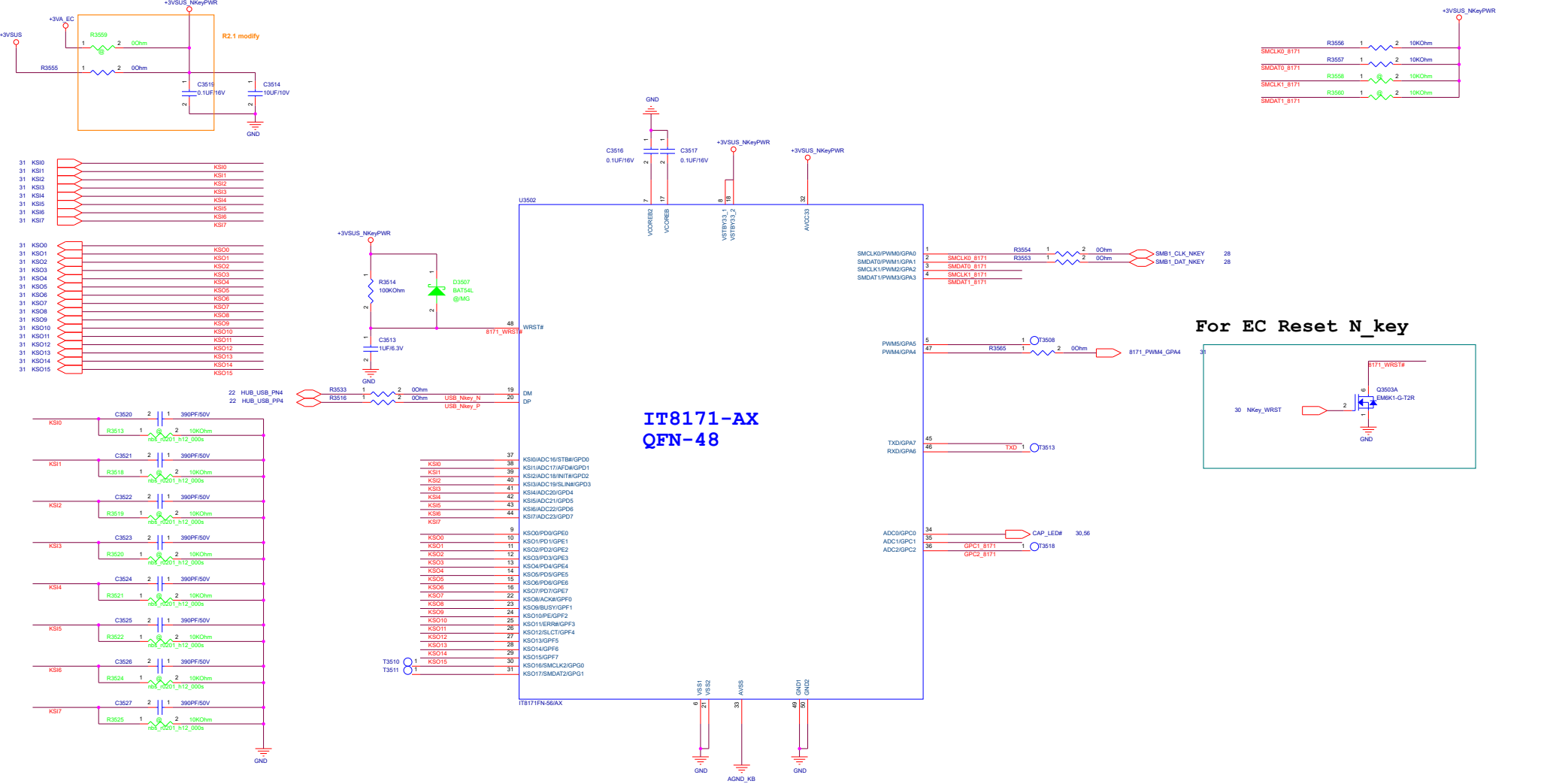


GND_LAN_T 上禁止加任何零件

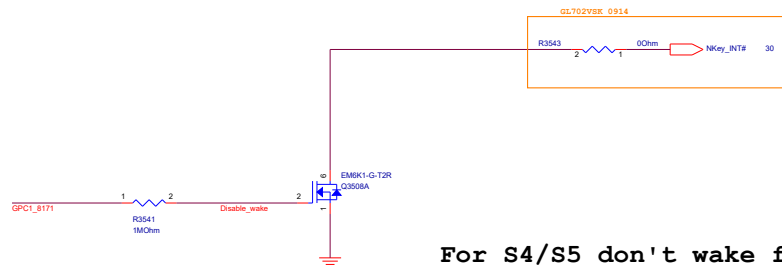
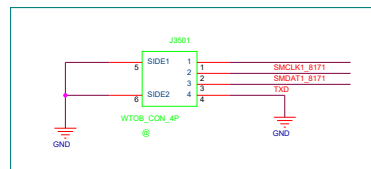
2012/2/16 EMI




Place near chassis GND



ITE 8171 debug con




For S4/S5 don't wake from KB

		Project Name	Rev
		GL702ZM	R1.0
Title : <Title>			
Size			
B	Dept.:	ASUSTeK COMPUTER INC. EE	Engineer: EE
Date:	Thursday, June 15, 2017	Sheet	29 of 102

<Variant Name>


<Variant Name>

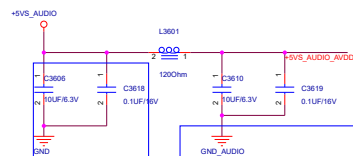
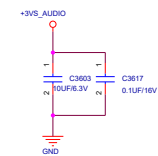
	Project Name GL702ZM	Rev R1.0
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Title : <Title>

Size A	Dept.: ASUSTeK COMPUTER INC. NB1	Engineer: EE
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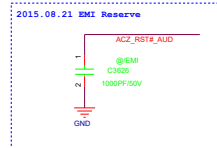
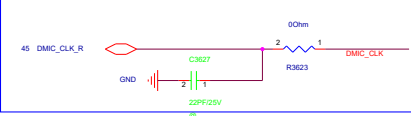
		Project Name	Rev
		GL702ZM	R1.0
Title : <Title>			
Size	Dept.: ASUSTeK COMPUTER INC. Engineer: EE		
A			
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R2,1-6 Rename C6513,2,C6514,2
Net name:GND to GND_AUDIO
Add C6528,C6527
C6513, ,C6514 close codec

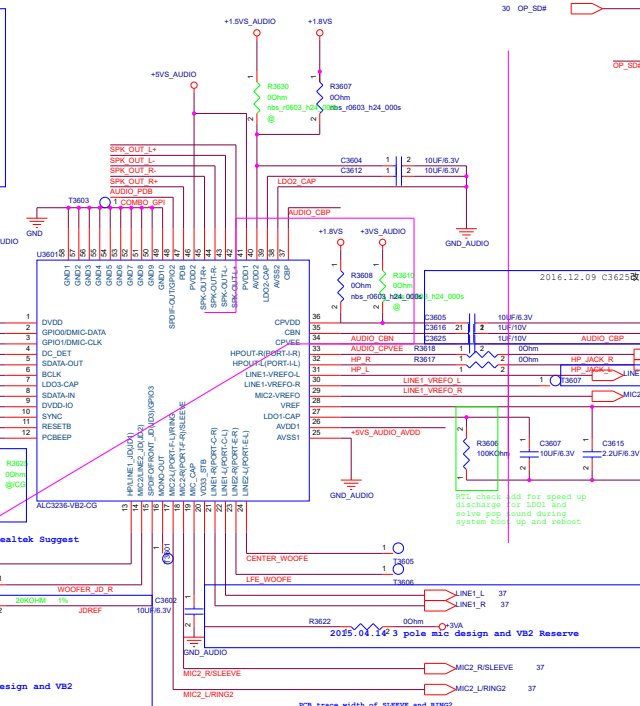
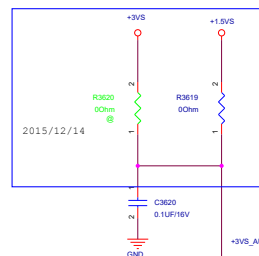
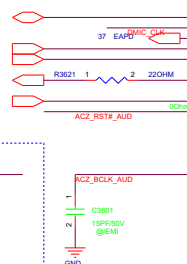
DIGITAL

R1.0_11 Add EMI Solution



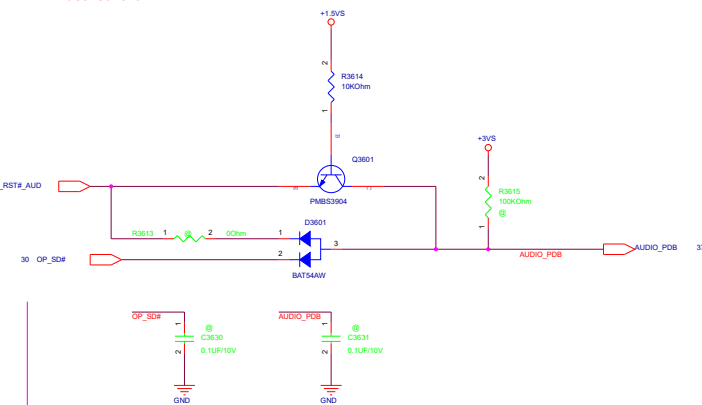
TO INTERNAL D-MIC

45 DMIC_DATA_R
5 ACZ_SDOUT_AUD
5 ACZ_BCLK_AUD
5 ACZ_SDOIN_AUD
5 ACZ_SYNC_AUD

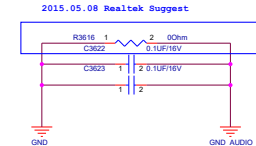


ANALOG

Mute control



2015.04.14 3 pole mic design and VB2 Reserve
2015.05.08 Realtek Suggest

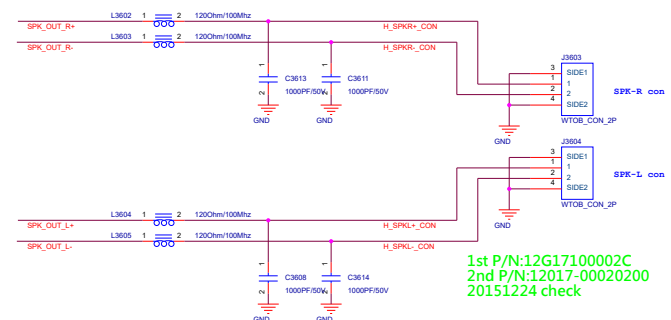
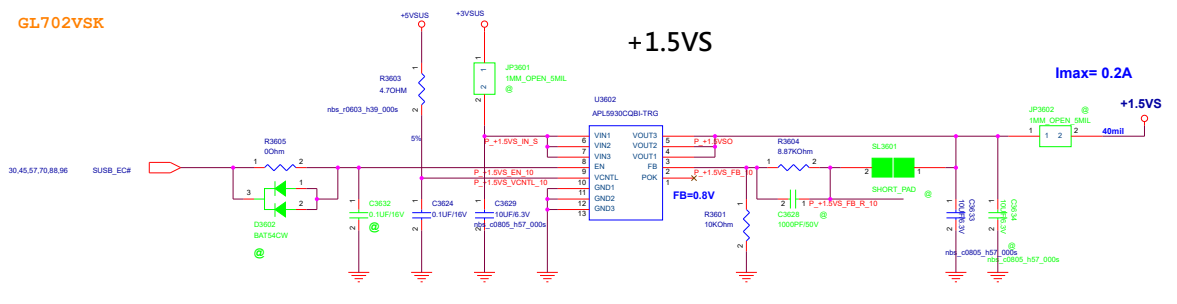


+1.5VS

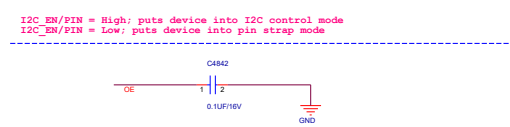
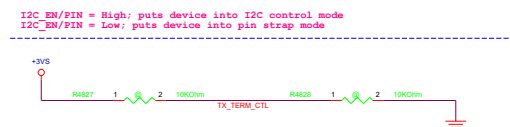
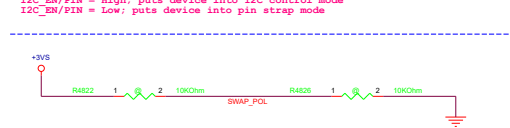
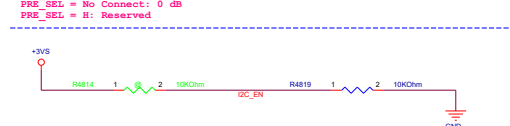
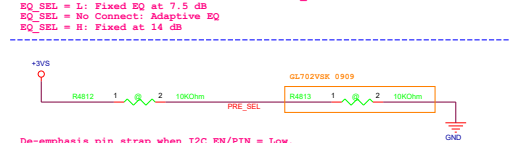
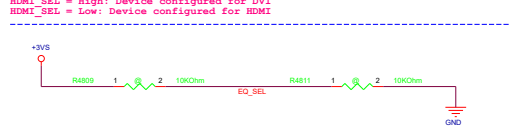
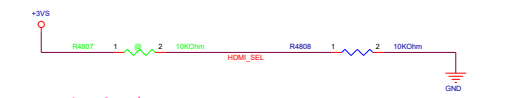
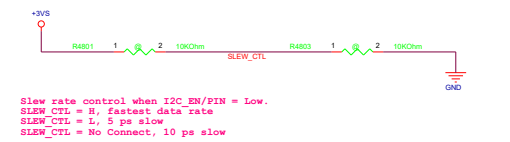
Imax = 0.2A

+1.5VS

GL702VSK

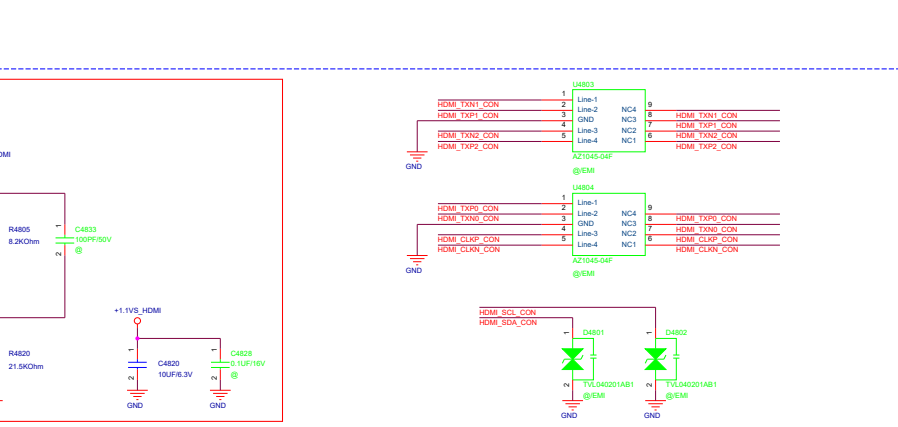
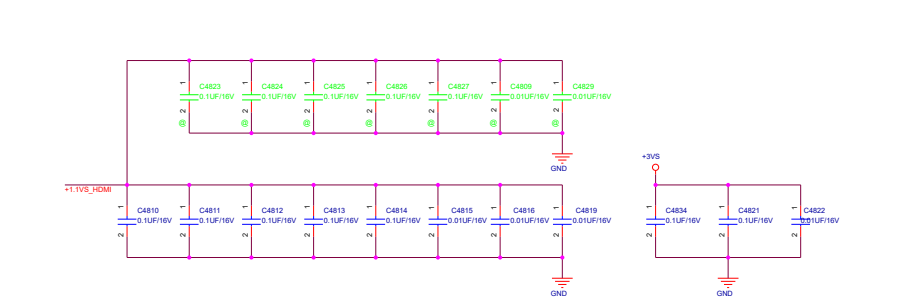
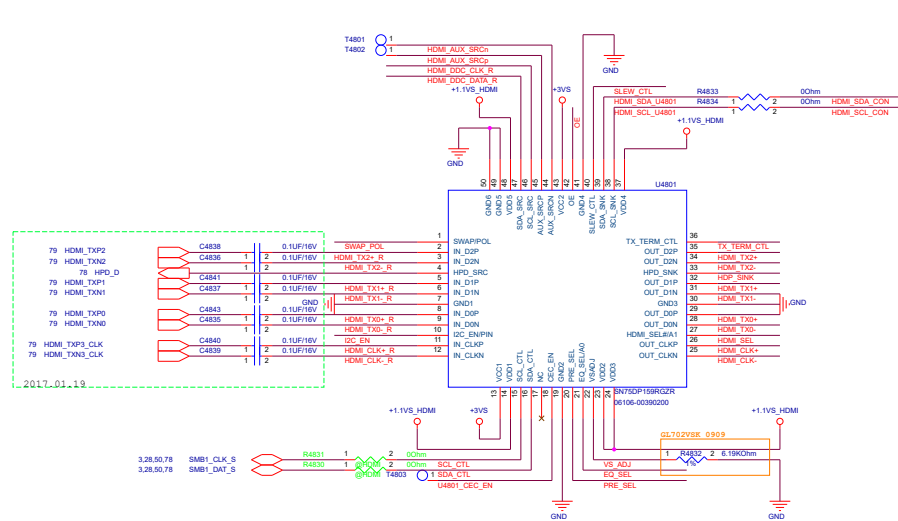
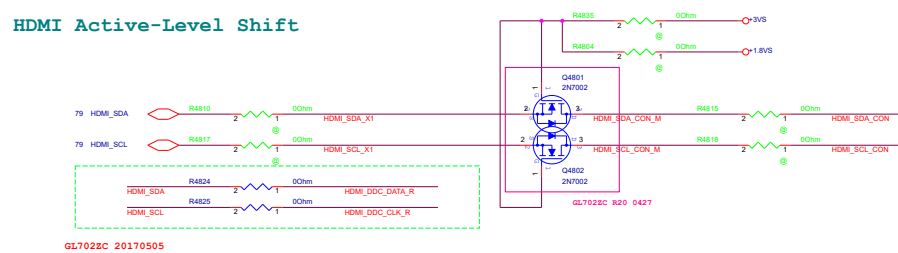


1st P/N:12G17100002C
2nd P/N:12017-00020200
20151224 check

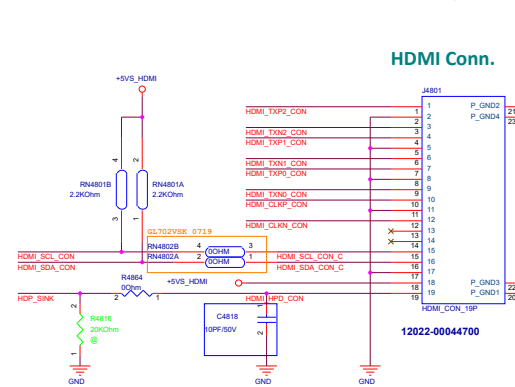
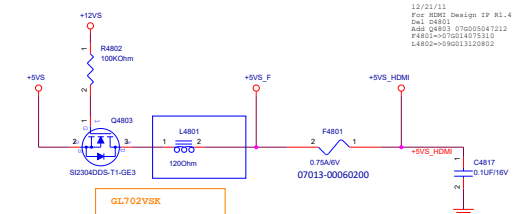


Operation enable/reset pin
 OE = L: Power-down mode OE = H: Normal operation
 Internal weak pullup: Resets device when transitions from H to L

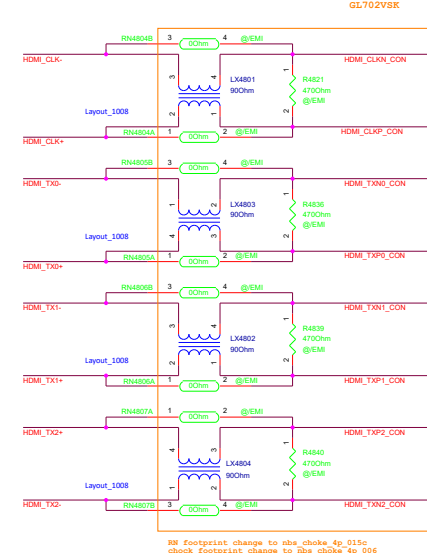
HDMI Active-Level Shift



HDMI PWR_+5VS_HDMI



HDMI EMI

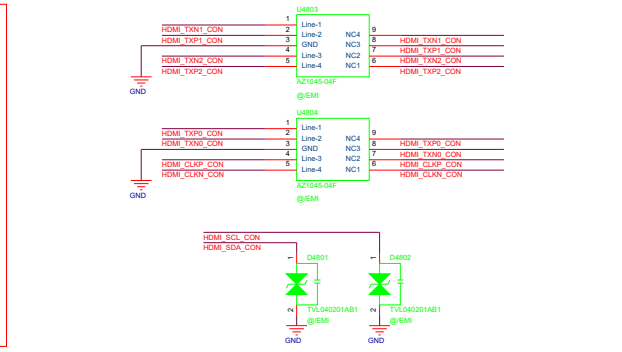
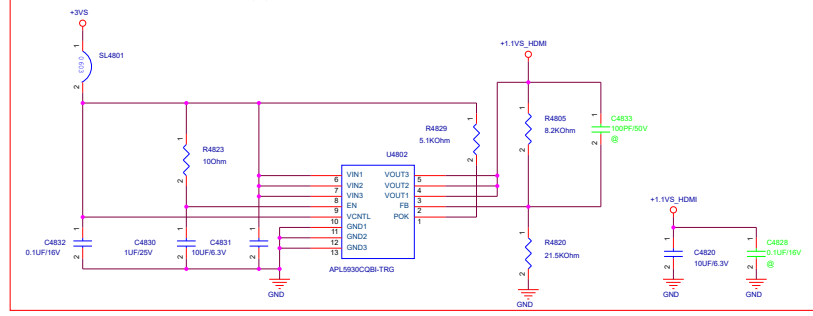


SW footprint change to the choke 4p_010c
 choke footprint change to 4ba_choke_4p_006

N56V C.M Choke : M 09G092090110

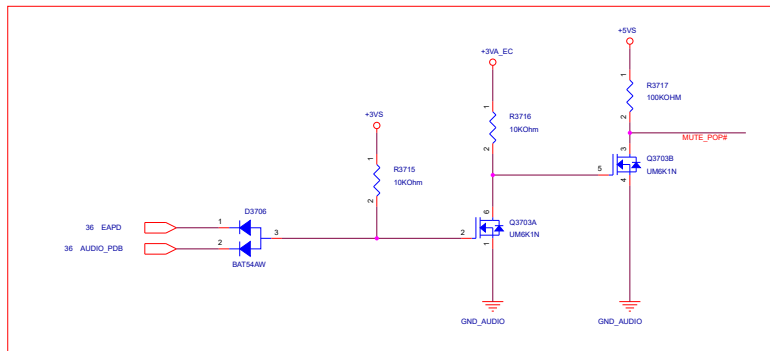
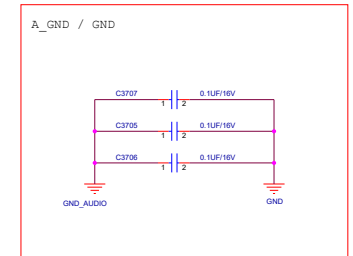
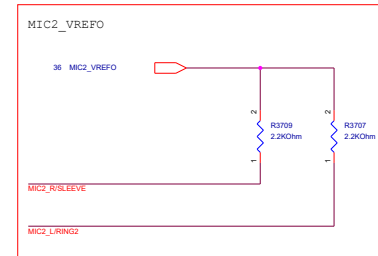
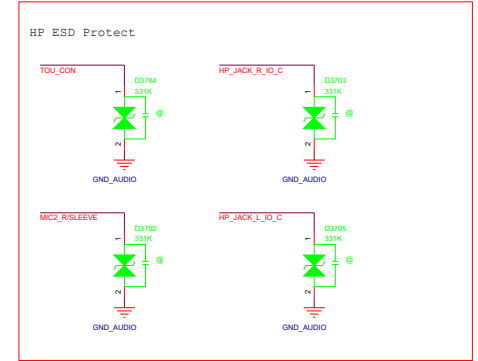
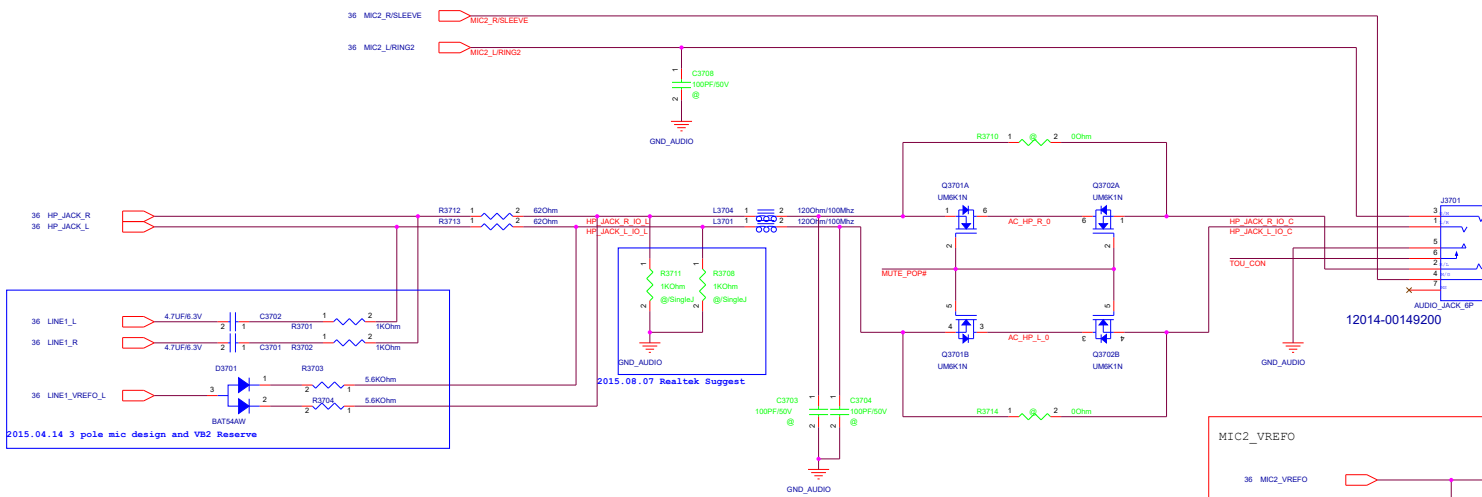
HDMI LDO 1.1VS

2016/4/21 R 1.4 1




Headphone&MIC

HP & MIC Connector



<Variant Name>

<Variant Name>


	Project Name GL702ZM	Rev R1.0
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Title : <Title>


Size Custom	Dept.: ASUSTeK COMPUTER INC. NB1	Engineer: EE
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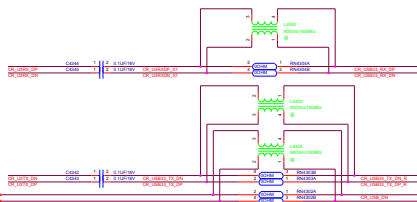
Date: Thursday, June 15, 2017	Sheet 49 of 102
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<Variant Name>

		Project Name		Rev
		GL702ZM		R1.0
Title : <Title>				
Size C	Dept.: ASUSTeK COMPUTER INC. NB1		Engineer:	EE
Date: Thursday, June 15, 2017			Sheet 42	of 102

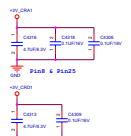
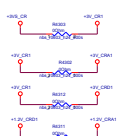
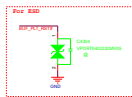
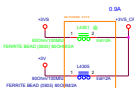
<Variant Name>

		Project Name		Rev
		GL702ZM		R1.0
Title : <Title>				
Size C	Dept.: ASUSTeK COMPUTER INC. NB1		Engineer:	EE
Date: Thursday, June 15, 2017			Sheet 54	of 102

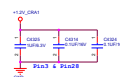


USB2.0_7 For CR

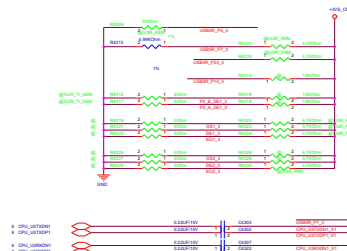
CardReader PWR



CR254, CR255 close to Pin23

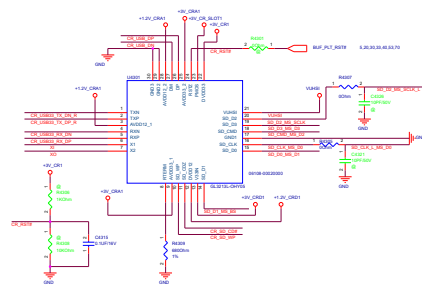
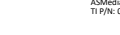


Close to J4301

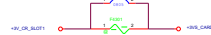


from APU

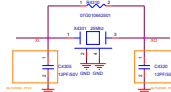
PARADE P/N: 06053-00320000(P58713)
ASMedia P/N: 02014-00020000
TI P/N: 06053-00080000



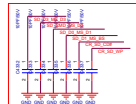
CR Socket



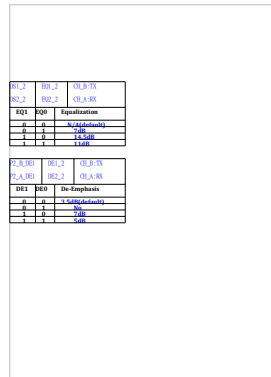
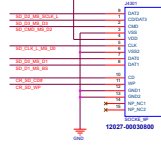
Reserved fuse for safety



X2001: 02002 <= Output 100V (220V)
1st: PIN 0700-00020100 EPS/ONPA-2180
2nd: PIN 0700-00020000 TAC/TV20000000



EMI 0134



Pin 1	Pin 2	Pin 3	Pin 4
Pin 5	Pin 6	Pin 7	Pin 8
Pin 9	Pin 10	Pin 11	Pin 12
Pin 13	Pin 14	Pin 15	Pin 16
Pin 17	Pin 18	Pin 19	Pin 20
Pin 21	Pin 22	Pin 23	Pin 24
Pin 25	Pin 26	Pin 27	Pin 28
Pin 29	Pin 30	Pin 31	Pin 32
Pin 33	Pin 34	Pin 35	Pin 36
Pin 37	Pin 38	Pin 39	Pin 40
Pin 41	Pin 42	Pin 43	Pin 44
Pin 45	Pin 46	Pin 47	Pin 48
Pin 49	Pin 50	Pin 51	Pin 52
Pin 53	Pin 54	Pin 55	Pin 56
Pin 57	Pin 58	Pin 59	Pin 60
Pin 61	Pin 62	Pin 63	Pin 64
Pin 65	Pin 66	Pin 67	Pin 68
Pin 69	Pin 70	Pin 71	Pin 72
Pin 73	Pin 74	Pin 75	Pin 76
Pin 77	Pin 78	Pin 79	Pin 80
Pin 81	Pin 82	Pin 83	Pin 84
Pin 85	Pin 86	Pin 87	Pin 88
Pin 89	Pin 90	Pin 91	Pin 92
Pin 93	Pin 94	Pin 95	Pin 96
Pin 97	Pin 98	Pin 99	Pin 100

Pin 1 Pin 2 Pin 3 Pin 4

Pin 5 Pin 6 Pin 7 Pin 8

Pin 9 Pin 10 Pin 11 Pin 12

Pin 13 Pin 14 Pin 15 Pin 16

Pin 17 Pin 18 Pin 19 Pin 20

Pin 21 Pin 22 Pin 23 Pin 24

Pin 25 Pin 26 Pin 27 Pin 28

Pin 29 Pin 30 Pin 31 Pin 32

Pin 33 Pin 34 Pin 35 Pin 36

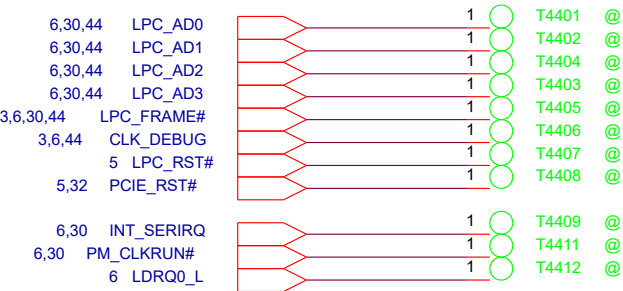
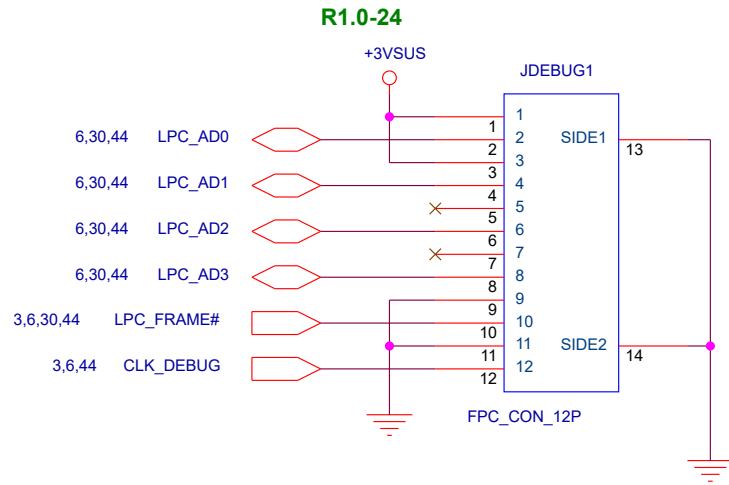
Pin 37 Pin 38 Pin 39 Pin 40

Pin 41 Pin 42 Pin 43 Pin 44

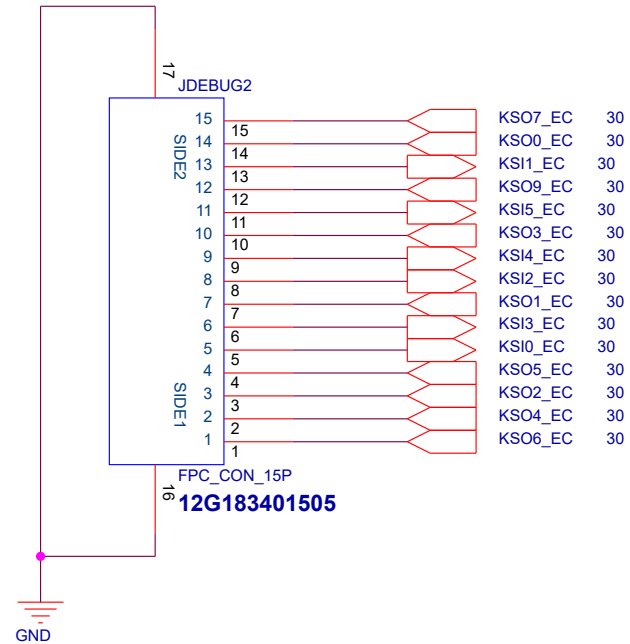
Pin 45 Pin 46 Pin 47 Pin 48

Pin 49 Pin 50 Pin 51 Pin 52

LPC Debug Port



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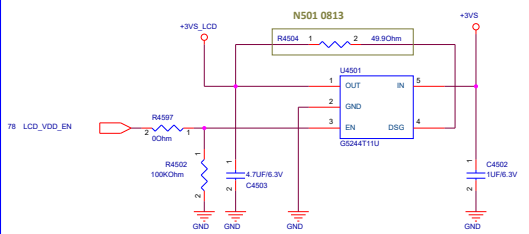


<Variant Name>

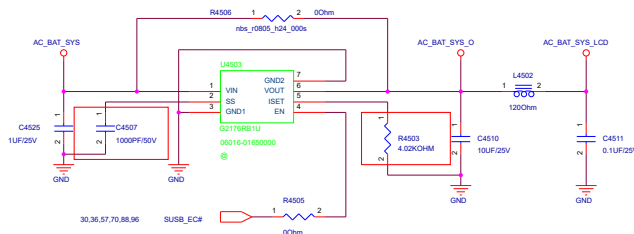
ASUS		Project Name	Rev
		GL702ZM	R1.0
Title : DEBUG_LPC			
Size A	Dept.: ASUSTeK COMPUTER INC. Engineer: EE		
Date: Thursday, June 15, 2017	Sheet	44	of 102

<Variant Name>

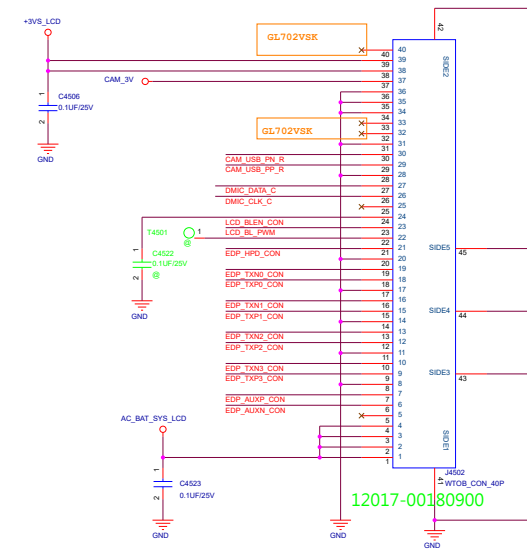
LCD Power switch



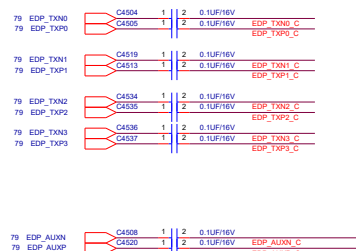
Panel BL Power



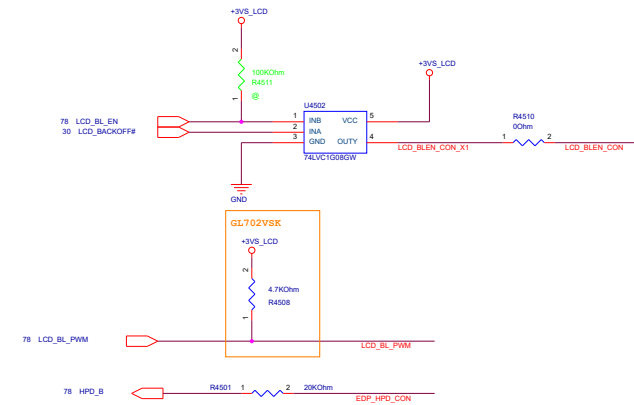
eDP Panel Conn.



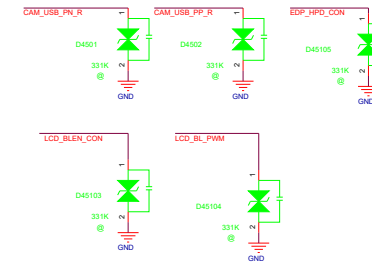
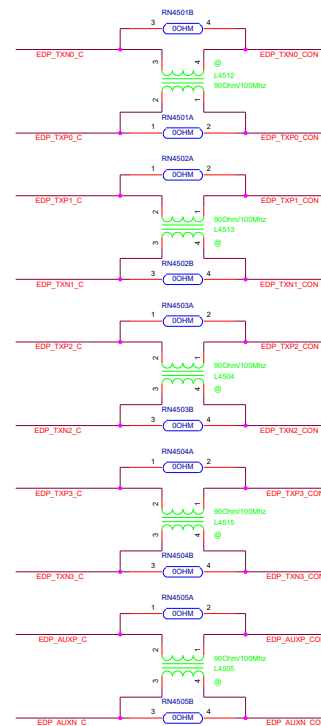
eDP from CPU



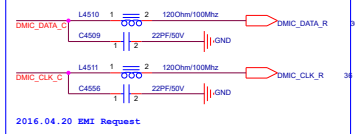
Panel



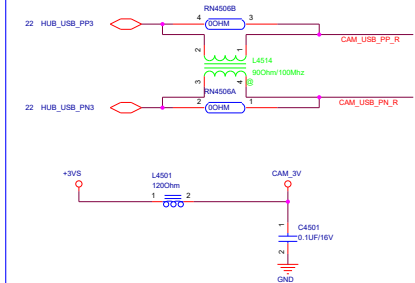
For EMI



MIC




Camera module



<Variant Name>

<Variant Name>


	Project Name GL702ZM	Rev R1.0
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Title : <Title>
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Size Custom	Dept.: ASUSTeK COMPUTER INC. NB1	Engineer: EE
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Date: Thursday, June 15, 2017	Sheet 66 of 102
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<Variant Name>

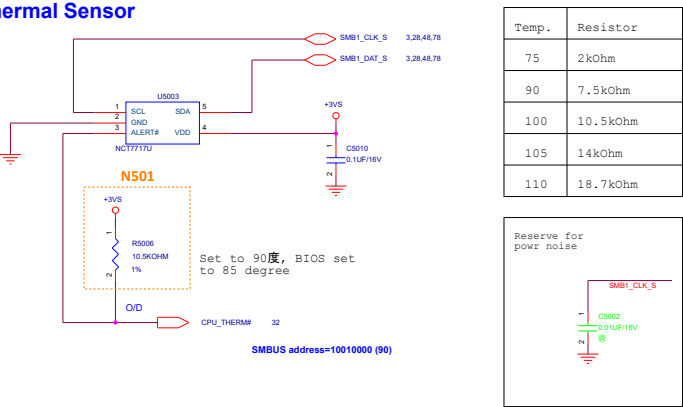
	Project Name GL702ZM	Rev R1.0
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Title : <Title>

Size Custom	Dept.: ASUSTeK COMPUTER INC. NB1	Engineer: EE
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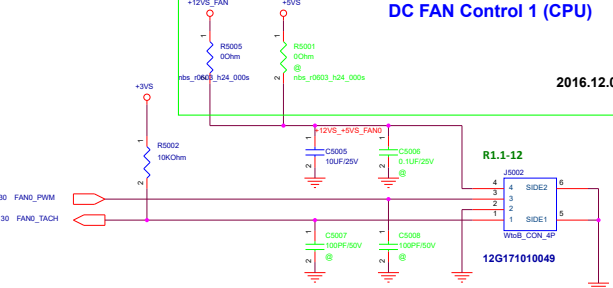
Date: Thursday, June 15, 2017	Sheet 68 of 102
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CPU Thermal Sensor



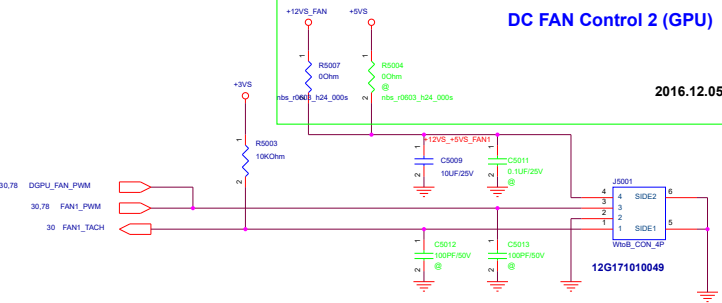
DC FAN Control 1 (CPU)

2016.12.05



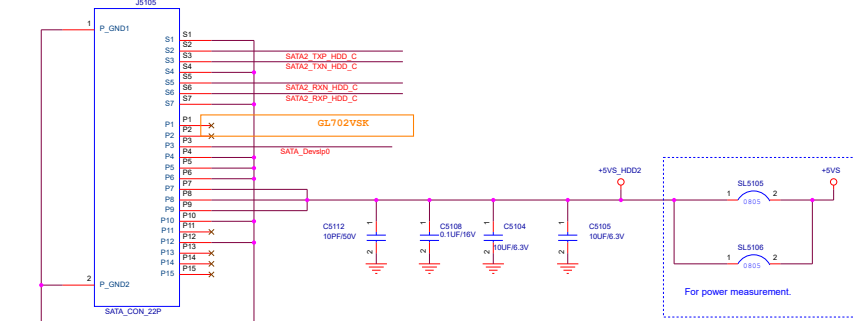
DC FAN Control 2 (GPU)

2016.12.05

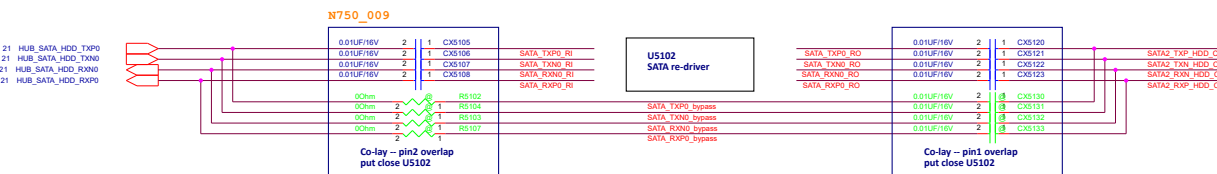
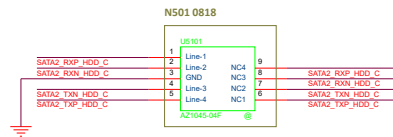
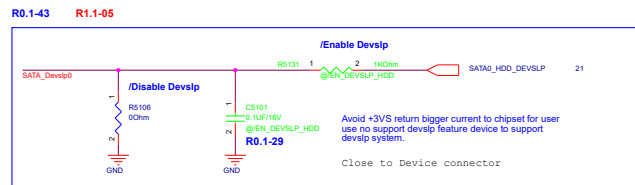


GL702VSK 0831

<Variant Name>

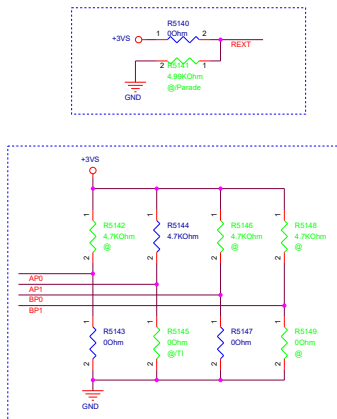


P/N:12015-00018300
20161213 check



SATA Re-driver for reserve 2nd HDD

267mW @3.3V



SATA3 Re-Driver : TI / SN75LVCP601RTJT

Vendor1: 06053-00110000 TI / SN75LVCP601RTJT

Vendor2: 06053-00450000 Asmedia / ASM1466

Optional
/TI : Need Mount in TI IC.

/ASM : Need Mount in Asmedia IC.

TI / SN75LVCP601

Function	Pin No.	Mount
PWR	10, 20	R5103, R5101
GND	18, 3, 13	R5130
Enable	7	R5152

Control Pin --Enable

TI & ASM Pin7

Mount R5153 = 0 : Device in StandBy mode.
Mount R5152 = 1 : Device enabled. (Default)

REXT

ASM Pin9

TI_Device Function

DEW_1 Pin 16	DEW_2 Pin 6	DE Width
0 Mount R5155	0 Mount R5151	SATA 3/2/1
1 Mount R5154	1 Mount R5150	SATA 2/1

TI_DE & EQ Settings

DE1 / DE2 Pin 8 / Pin 9	EQ1 / EQ2 Pin 17 / Pin 19	DE	EQ
NC Unmount R5110, Unmount R5108	NC Unmount R5111, Unmount R5109	-4 dB	0 dB
0 Mount R5110, Mount R5108	0 Mount R5111, Mount R5109	0 dB	7 dB
1 Mount R5106, Mount R5104	1 Mount R5107, Mount R5105	-2 dB	14 dB

Asmedia / ASM1466

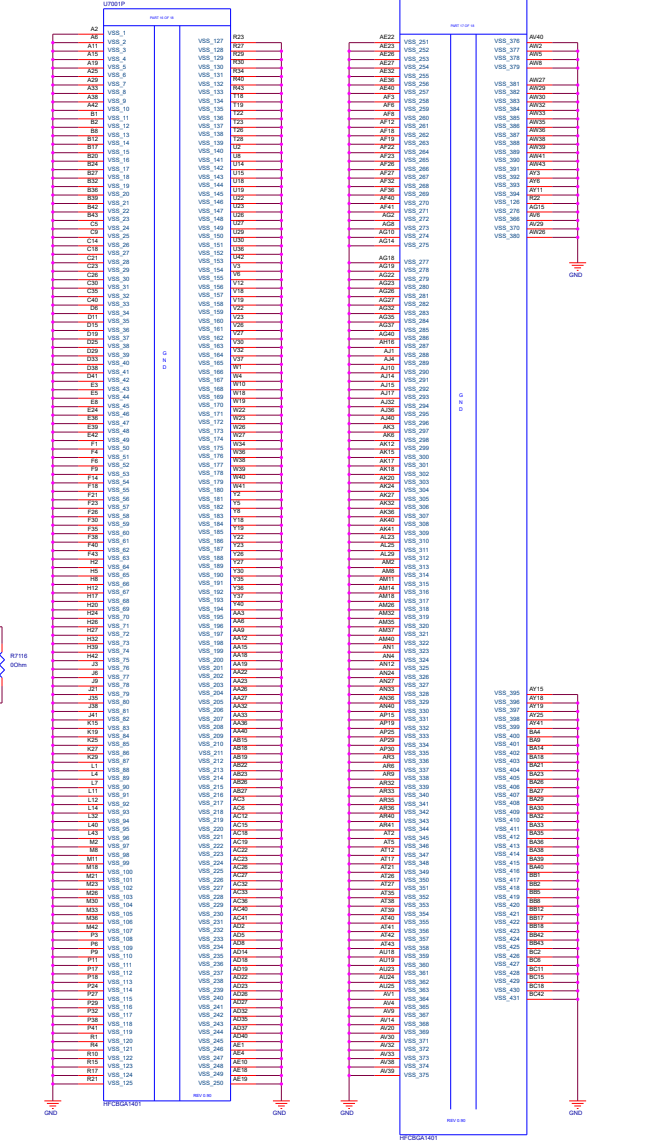
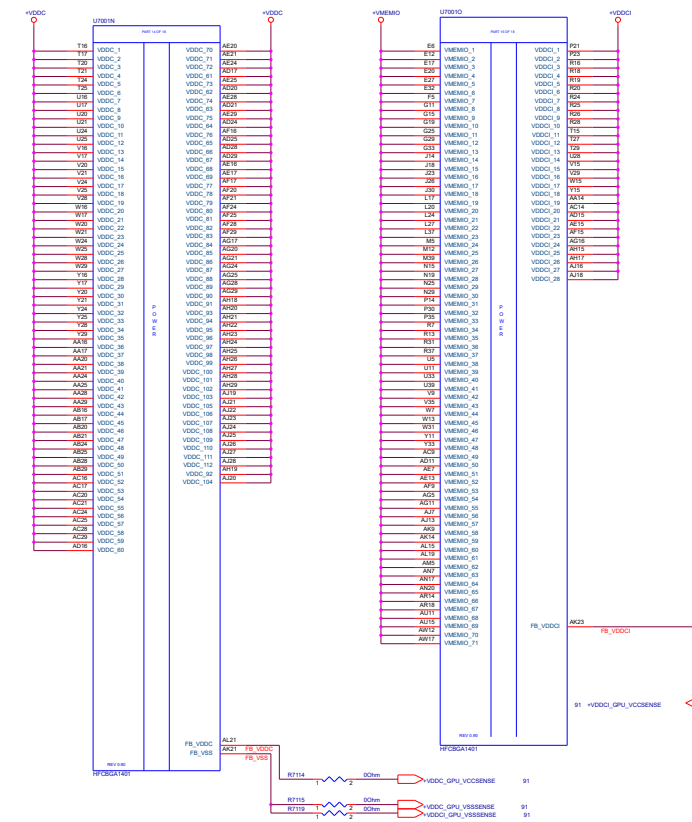
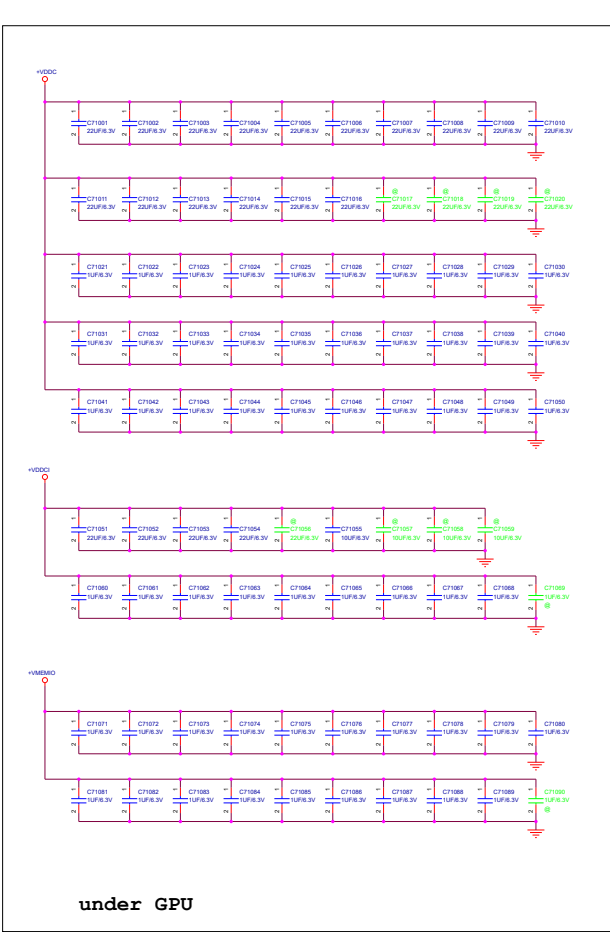
Function	Pin No.	Mount
PWR	6, 10, 16, 20	R5150, R5103, R5154, R5101
SMB BUS	18, 19	R5131, R5105
Enable	7	R5152
REXT	9	R5157

Asmedia_DE_X Settings

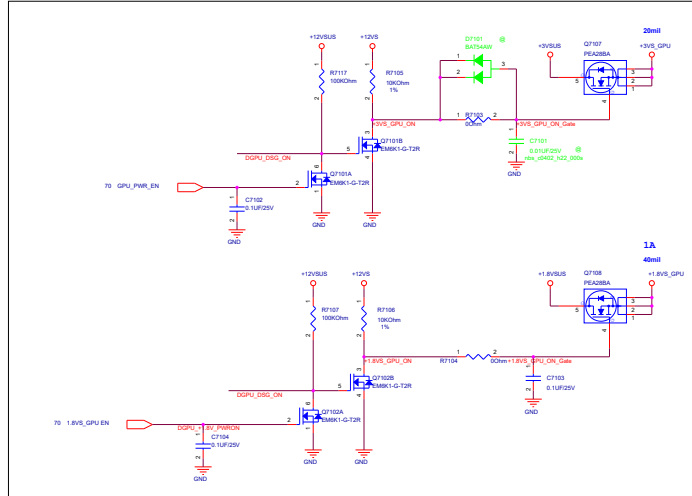
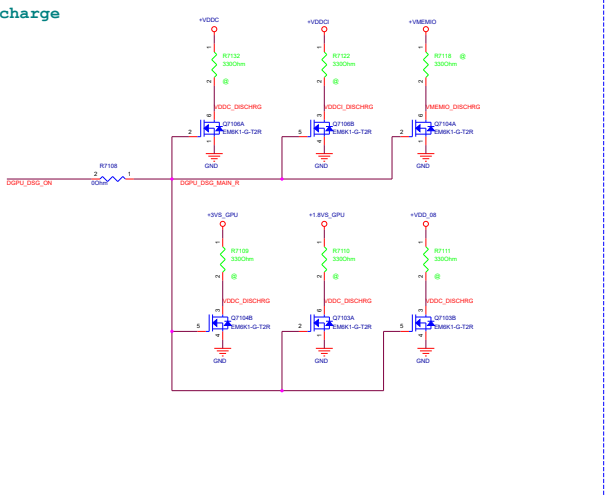
DE_A Pin 17	DE_B Pin 8	Driving
0 Mount R5111	0 Mount R5110	+1.5 dB
1 Mount R5107	1 Mount R5106	+3.0 dB

N750_003

<Variant Name>



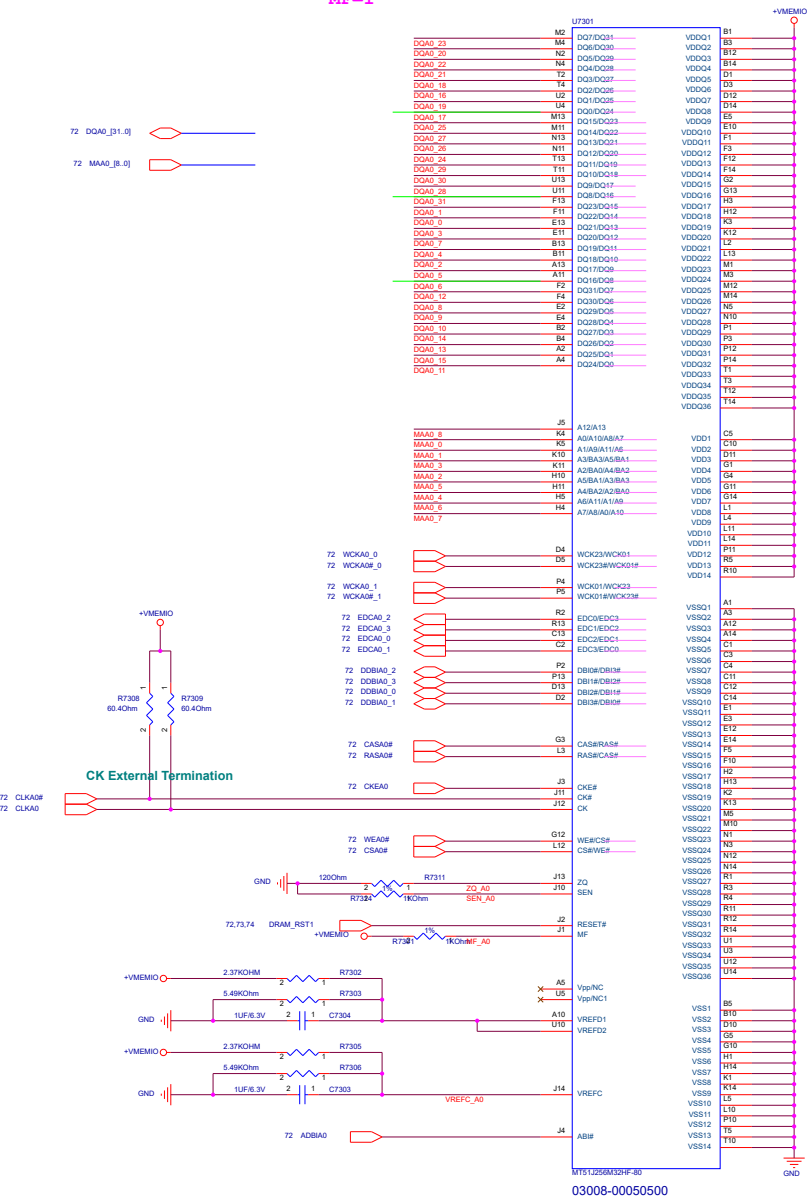
Discharge



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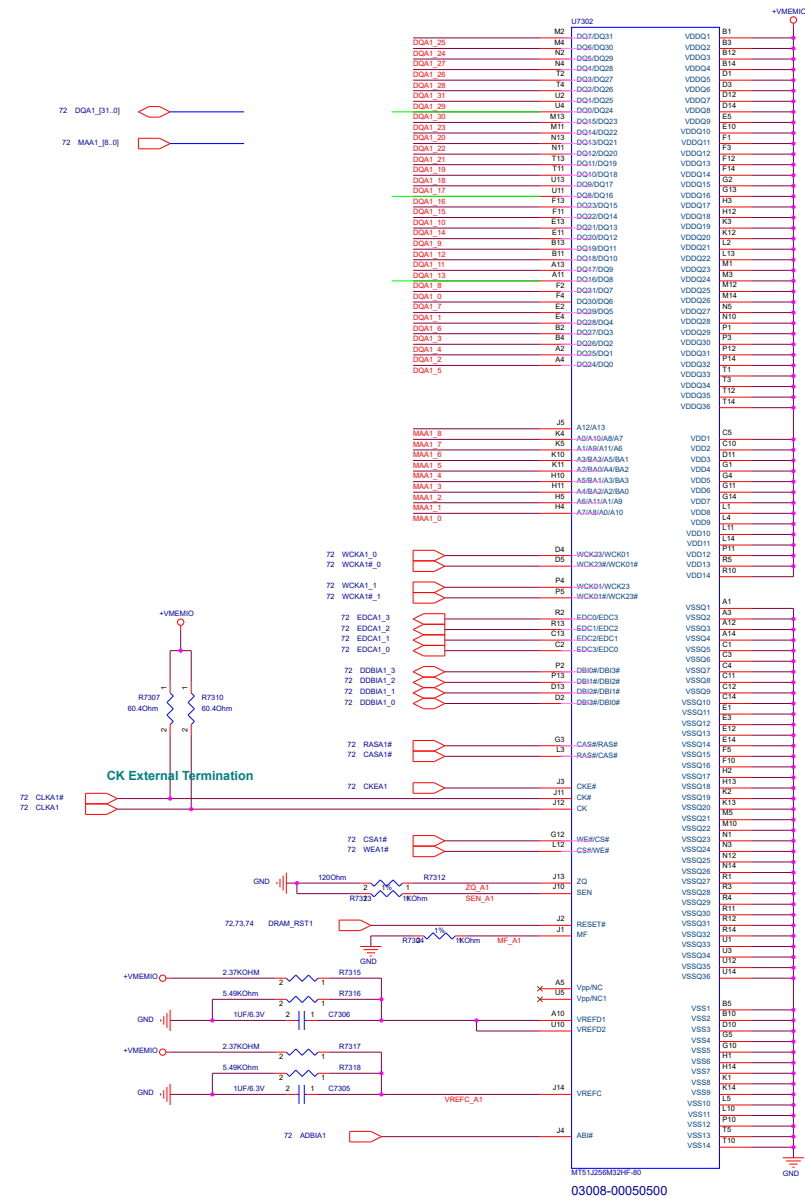
FBA Partition Memory (1 of 2)

MF=1



FBA Partition Memory (2 of 2)

MF=0 Normal




R1.3-02 R1.2-25

USE GDDR5 VRAM 128Mb x 32 (512MB)
 1st: P/N: 03008-00030100 HYNIX/H5GC4H24MFR-T2C (M-die), Strap: 0x2
 2nd: P/N: 03008-00030200 SAMSUNG/K4G41325FC-HC03, Strap: 0x3
 3rd: P/N: 03008-00030400 Micron/EDW4032BABG-60-F (B-die), Strap: 0x4

GDD5 MODE SELECTION

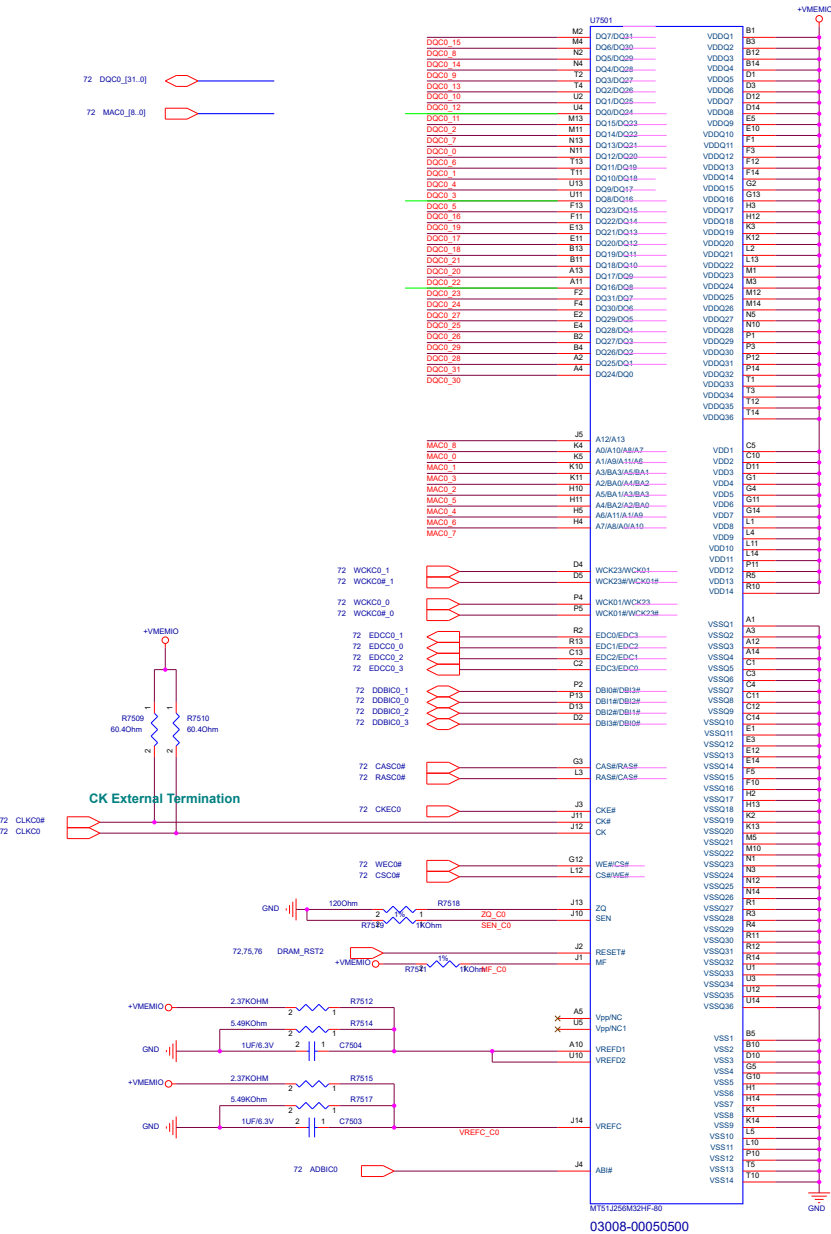
MODE	MF	EDC1	EDC2
x16	0	0	VDDQ
x32	0	VDDQ	VDDQ
x16 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ

<Variant Name>

		Project Name GL702ZM		Rev R1.0
Title : <Title>				
Size C	Dept.: ASUSTeK COMPUTER INC. NB1 Engineer: EE			
Date: Thursday, June 15, 2017			Sheet 64 of 102	

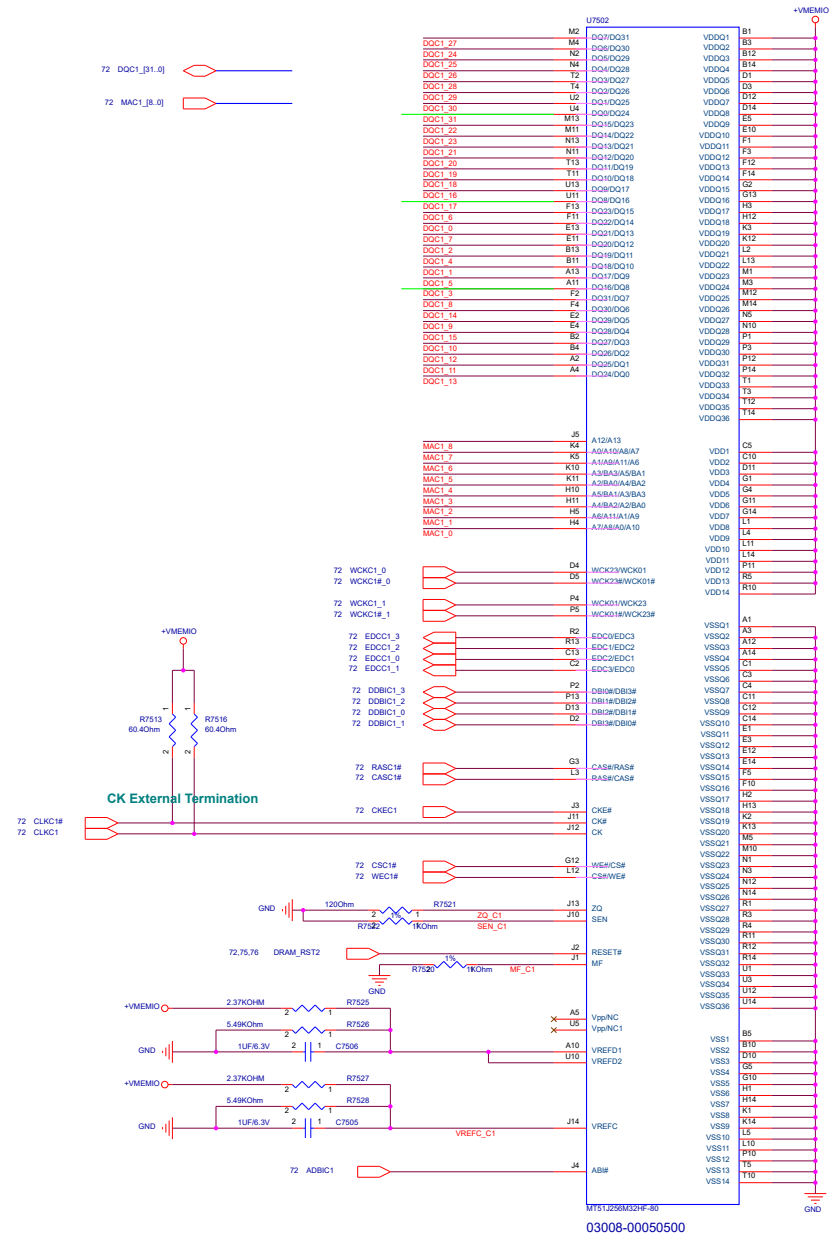
FBC Partition Memory (1 of 2)

MF=1 Mirror



FBC Partition Memory (2 of 2)

MF=0 Normal



R1.3-02 R1.2-25

USE GDDR5 VRAM 128Mb x32 (512MB)

1st: P/N:03008-00030100 HYNIX/H5GC4H24MFR-T2C (M-die), Strap: 0x2

2nd: P/N:03008-00030200 SAMSUNG/K4G4132FC-HC03, Strap: 0x3

3nd: P/N:03008-00030400 Micron/EDW4032BAG-60-F (B-die), Strap: 0x4

GDD5 MODE SELECTION

MODE	MF	EDC1	EDC2
x16	0	0	VDDQ
x32	0	VDDQ	VDDQ
x16 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ

<Variant Name>



Project Name

GL702ZM

Rev

R1.0

Title : **IO_HDT**

Size

C

Dept.:

ASUSTeK COMPUTER INC. NB1

Engineer:

EE

Date: **Thursday, June 15, 2017**

Sheet

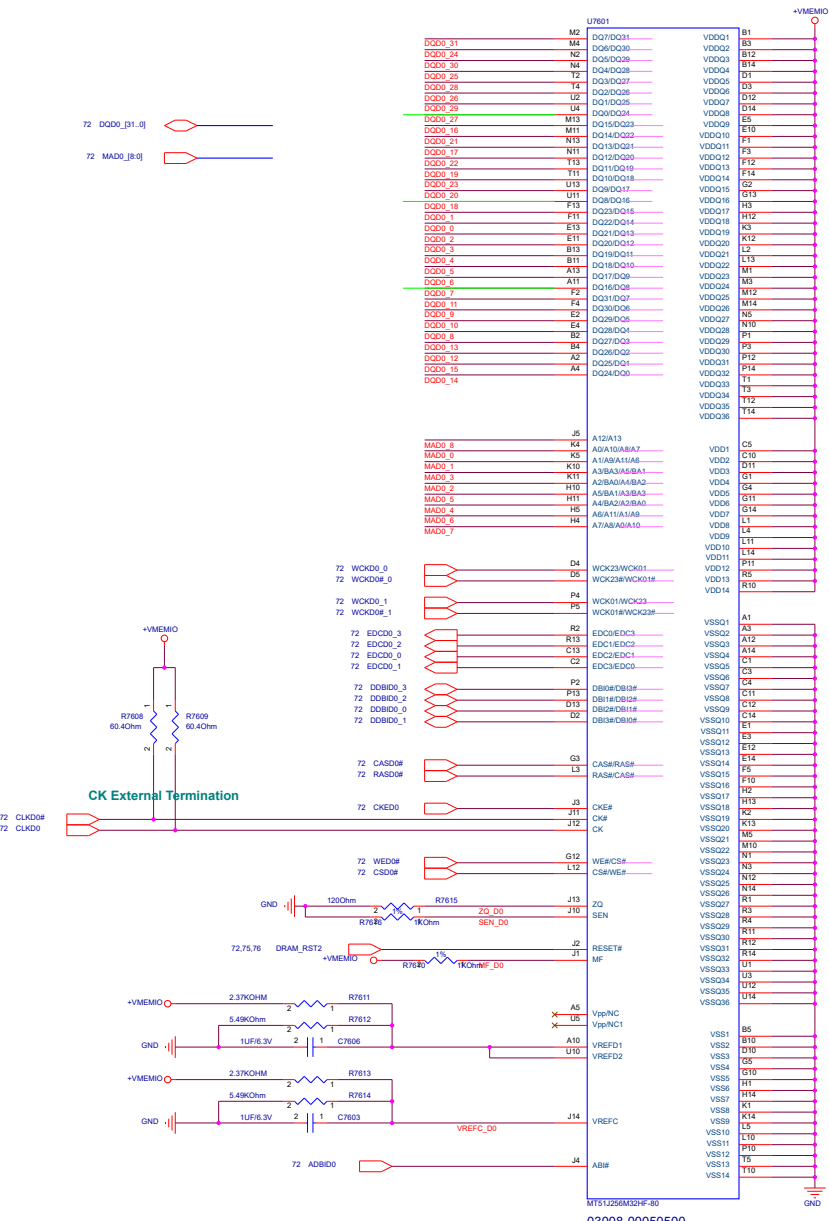
65

of

102

FBD Partition Memory (1 of 2)

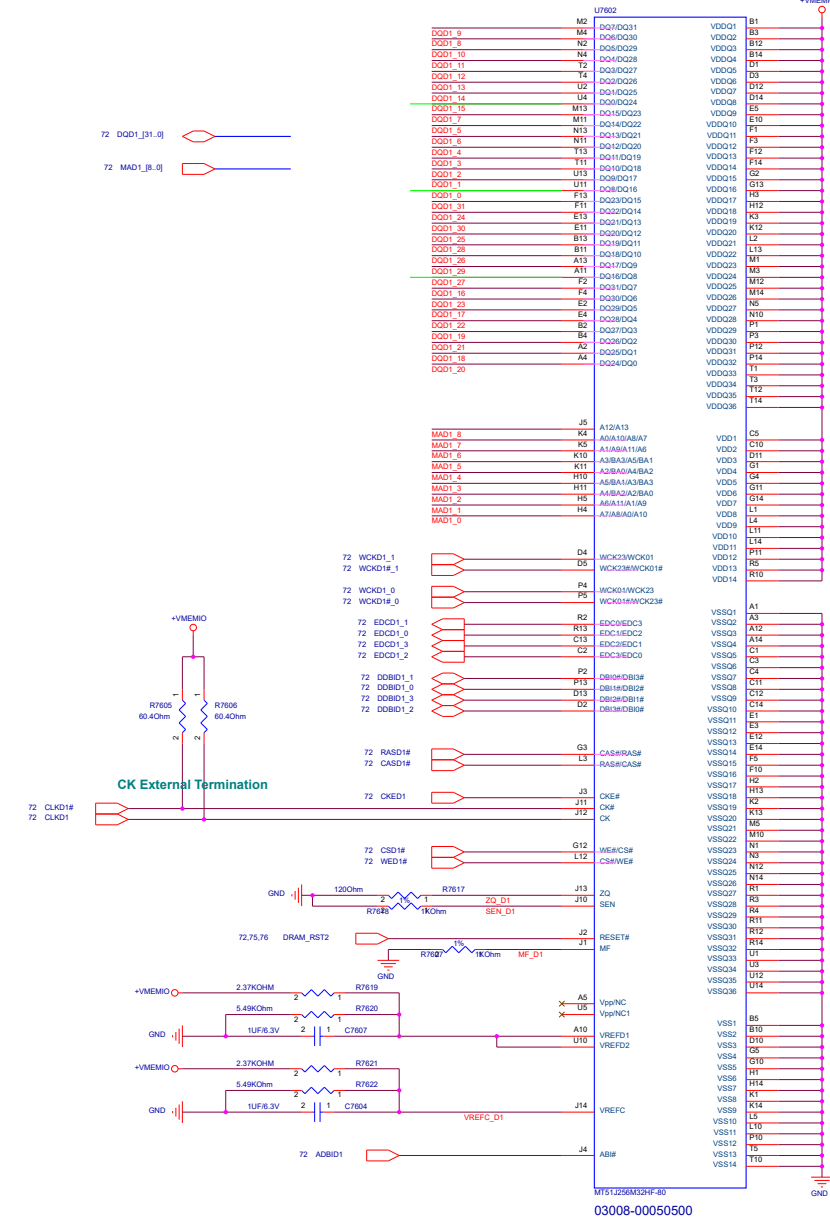
MF=1 Mirror



03008-00050500

FBD Partition Memory (2 of 2)

MF=0 Normal



03008-00050500

R1.3-02 R1.2-25

USE GDDR5 VRAM 128Mb x 32 (512MB)

1st: P/N:03008-00030100 HYNIX/HSGC4H24MFR-T2C (M-die),Strap: 0x2

2nd: P/N:03008-00030200 SAMSUNG/K4G41325F-C-HC03 ,Strap: 0x3

3nd: P/N:03008-00030400 Micron/EDW4032BAG-60-F (B-die),Strap: 0x4

GDDR5 MODE SELECTION

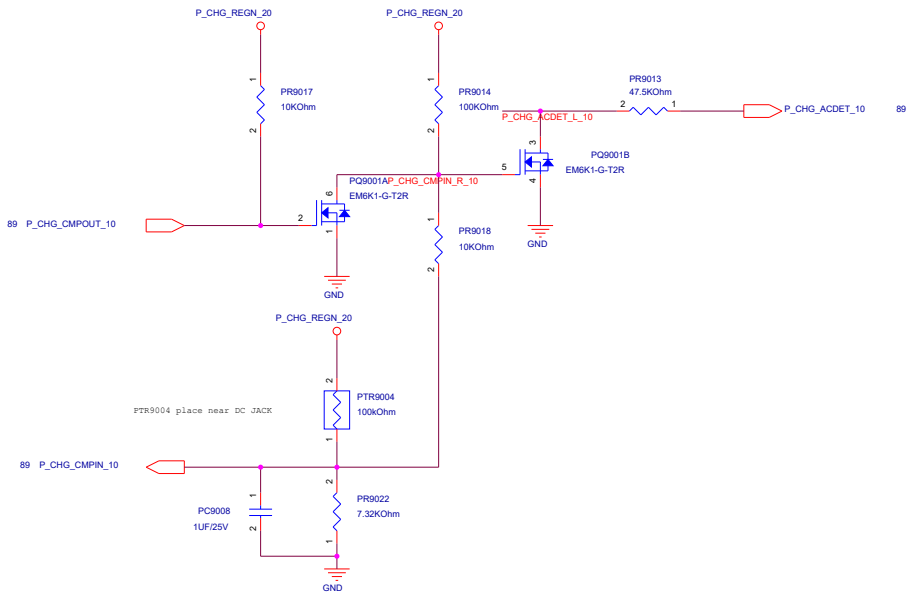
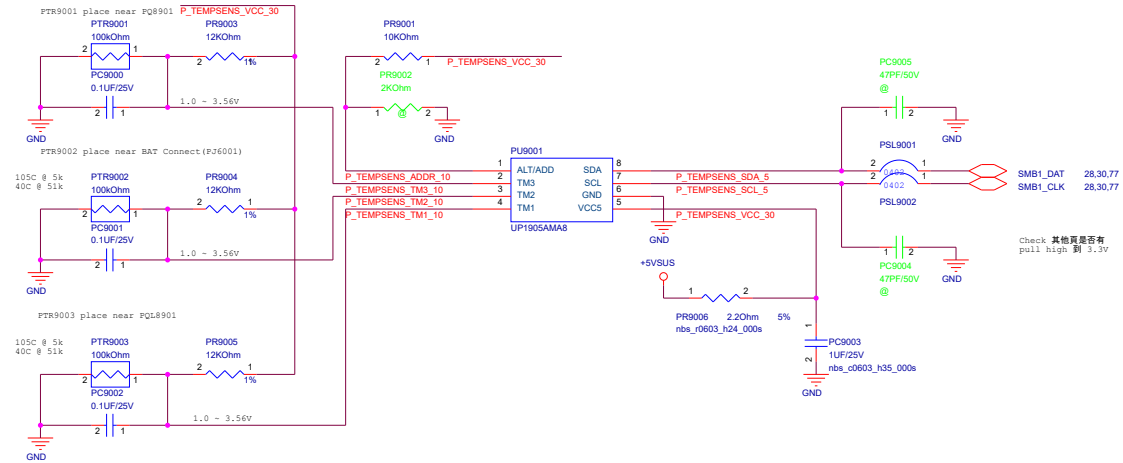
MODE	MF	EDC1	EDC2
x16	0	0	VDDQ
x32	0	VDDQ	VDDQ
x16 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ

Address Selection Table

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9001	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9002	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

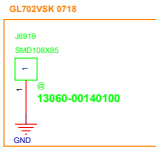
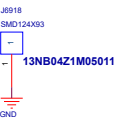
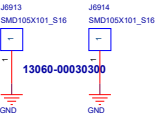
Register Address

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
R/W	W	W	W	R	R	R	R
Function	Temp. alert threshold setting			Sensed temp. data			bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert

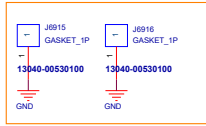


<Variant Name>

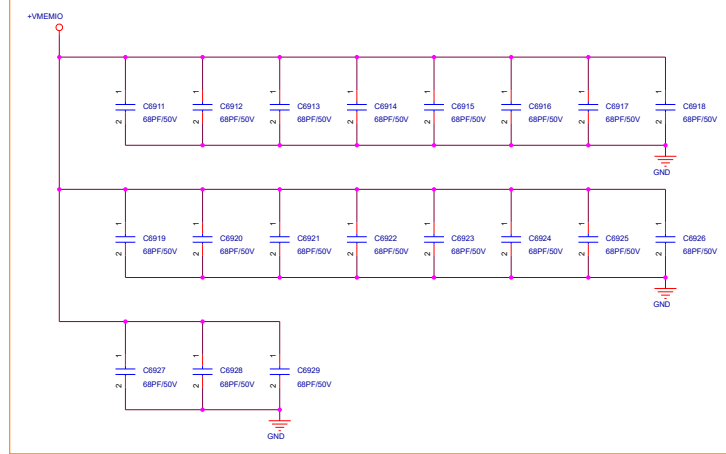
TOP side



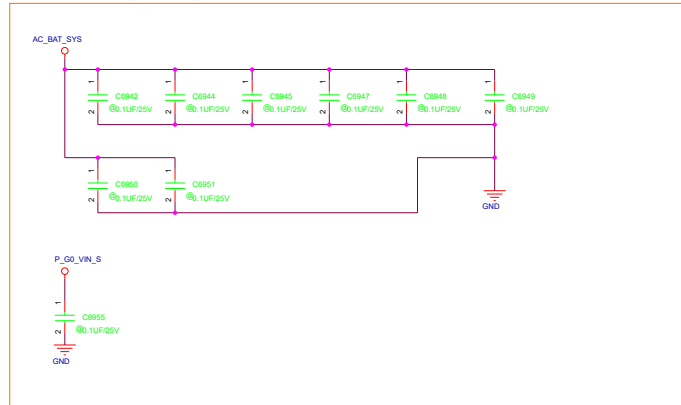
BOT side



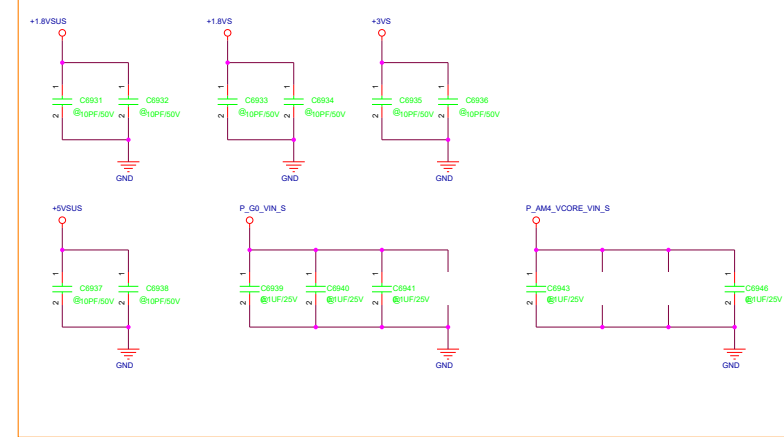
GL702VSK



GL702ZC EMI PR2 layout modify

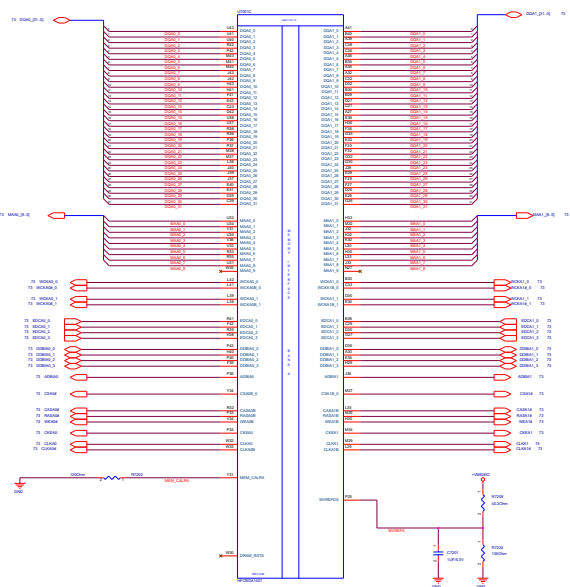


GL702ZC 20170510

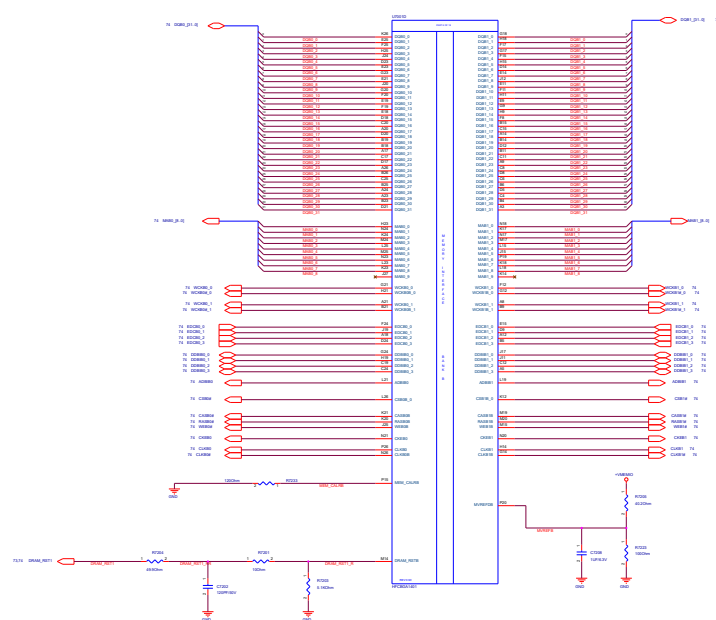


<Variant Name>

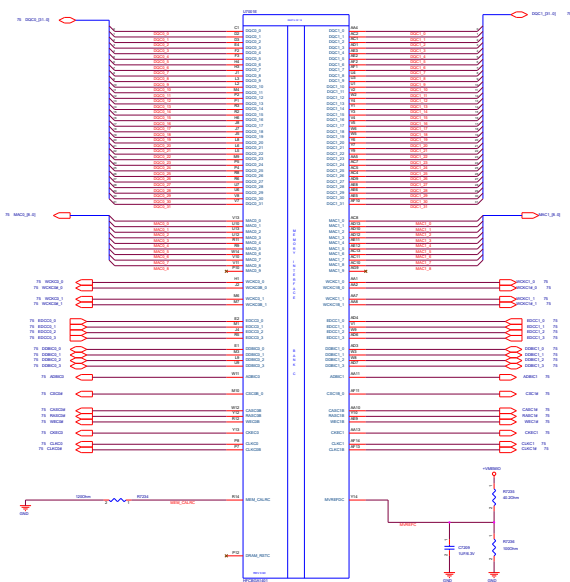
MEMORY: GPU FB Partition A



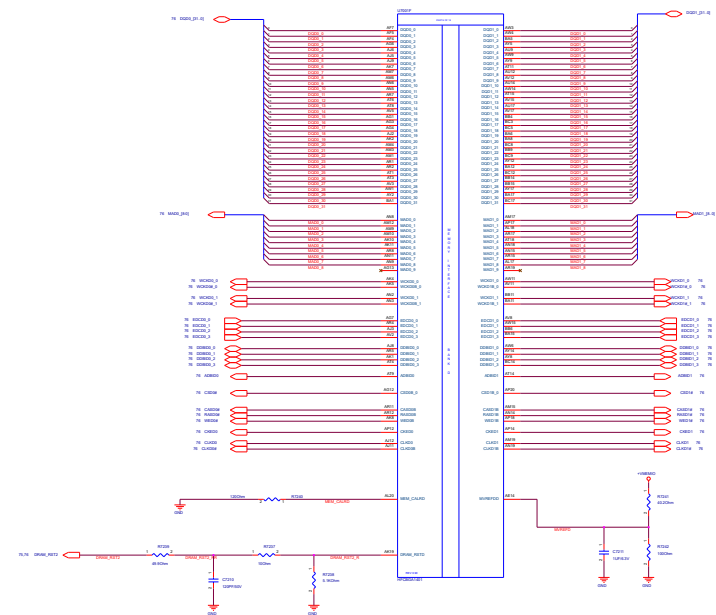
MEMORY: GPU FB Partition B



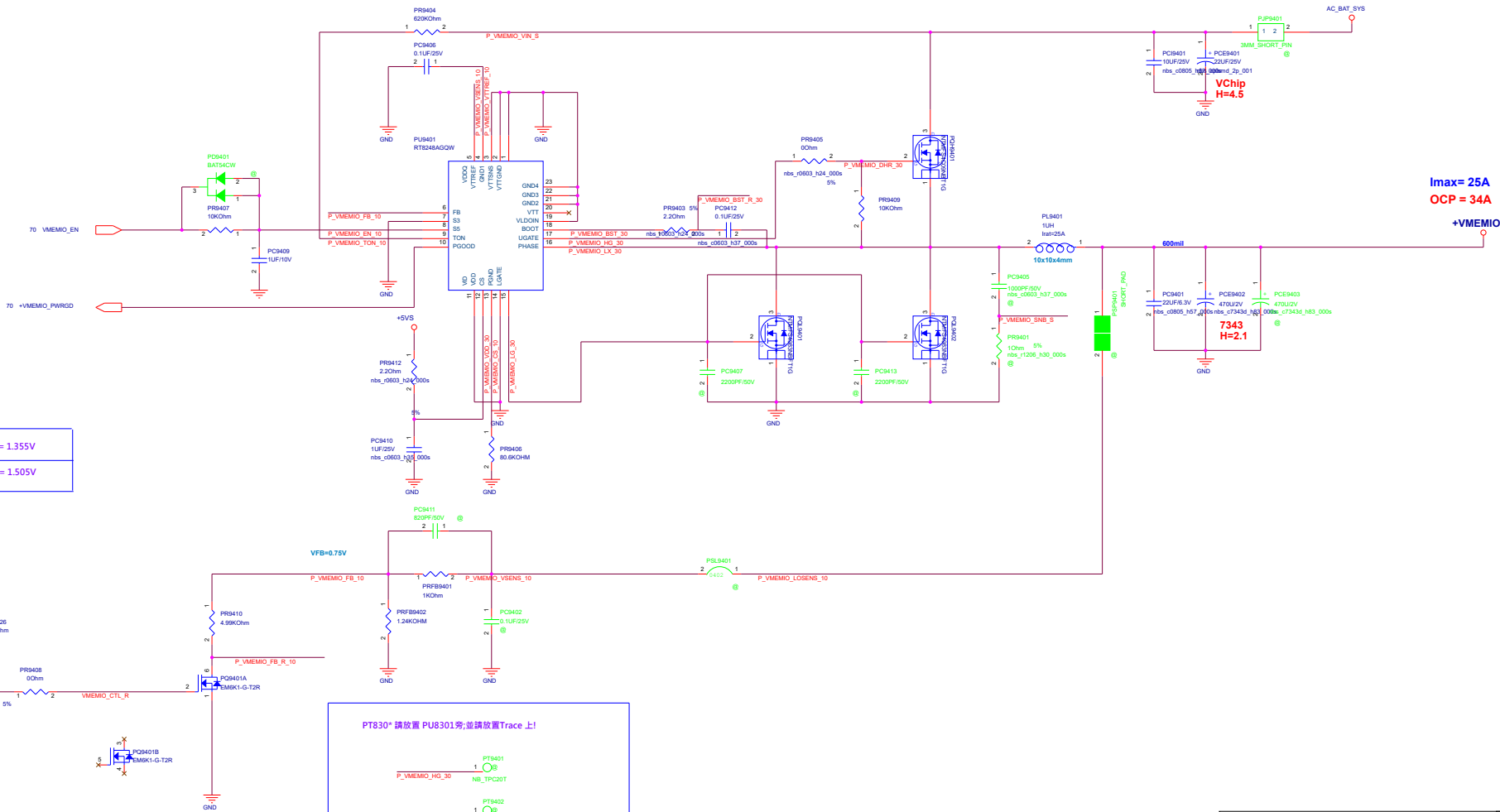
MEMORY: GPU FB Partition C




MEMORY: GPU FB Partition D




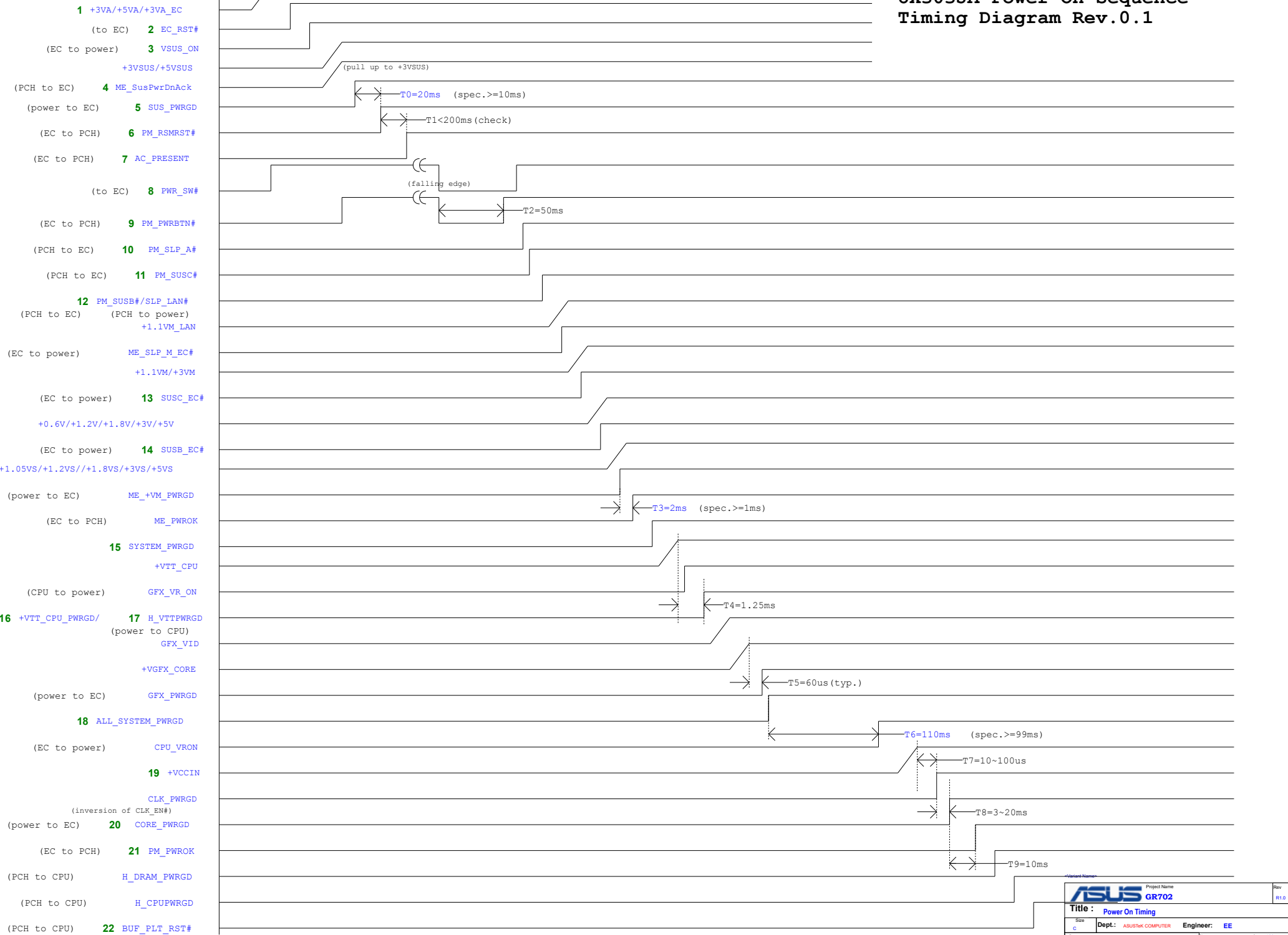
+ VMEMIO

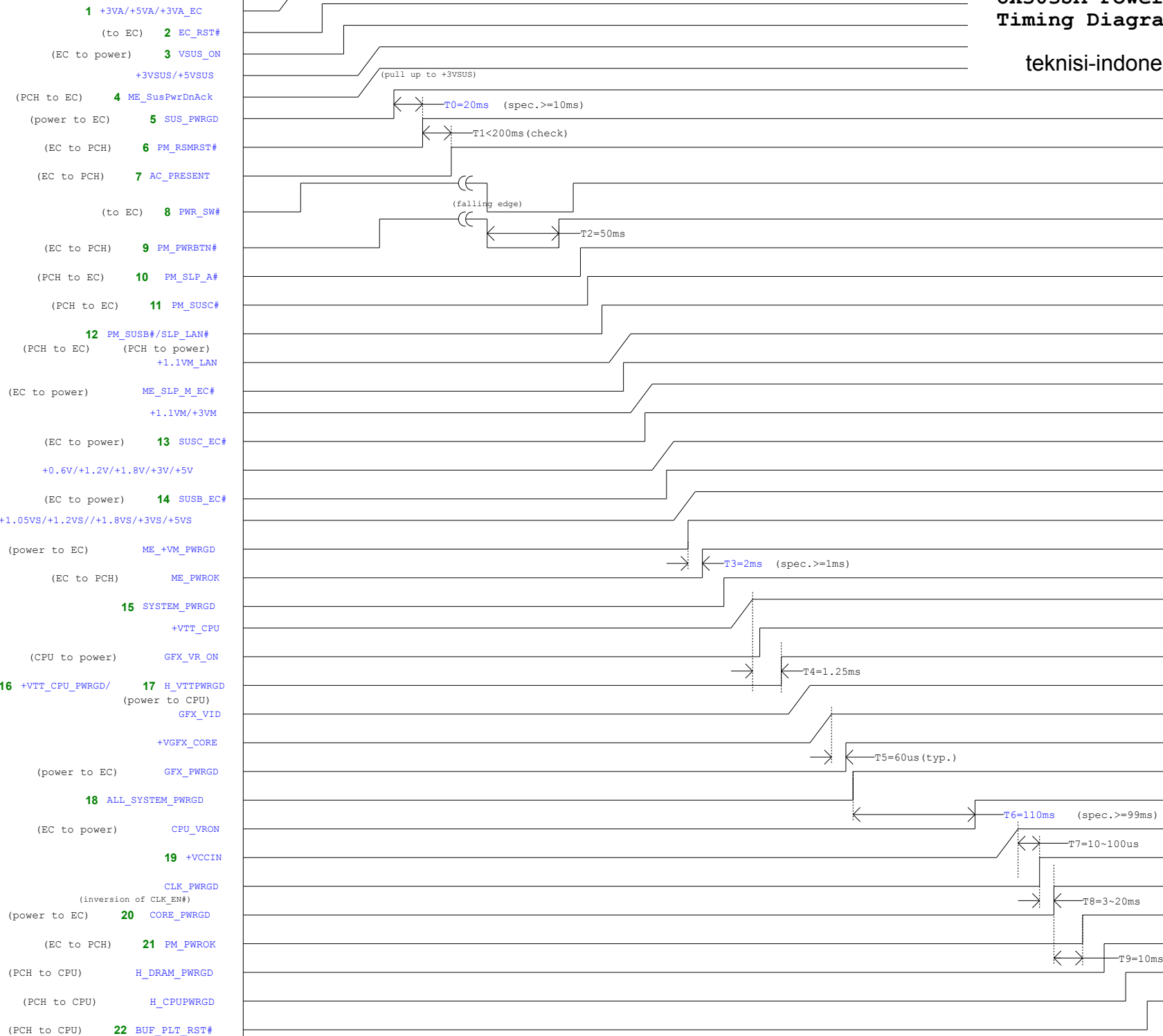


VMEMIO_CTL = Low	+VMEMIO = 1.355V
VMEMIO_CTL = High	+VMEMIO = 1.505V

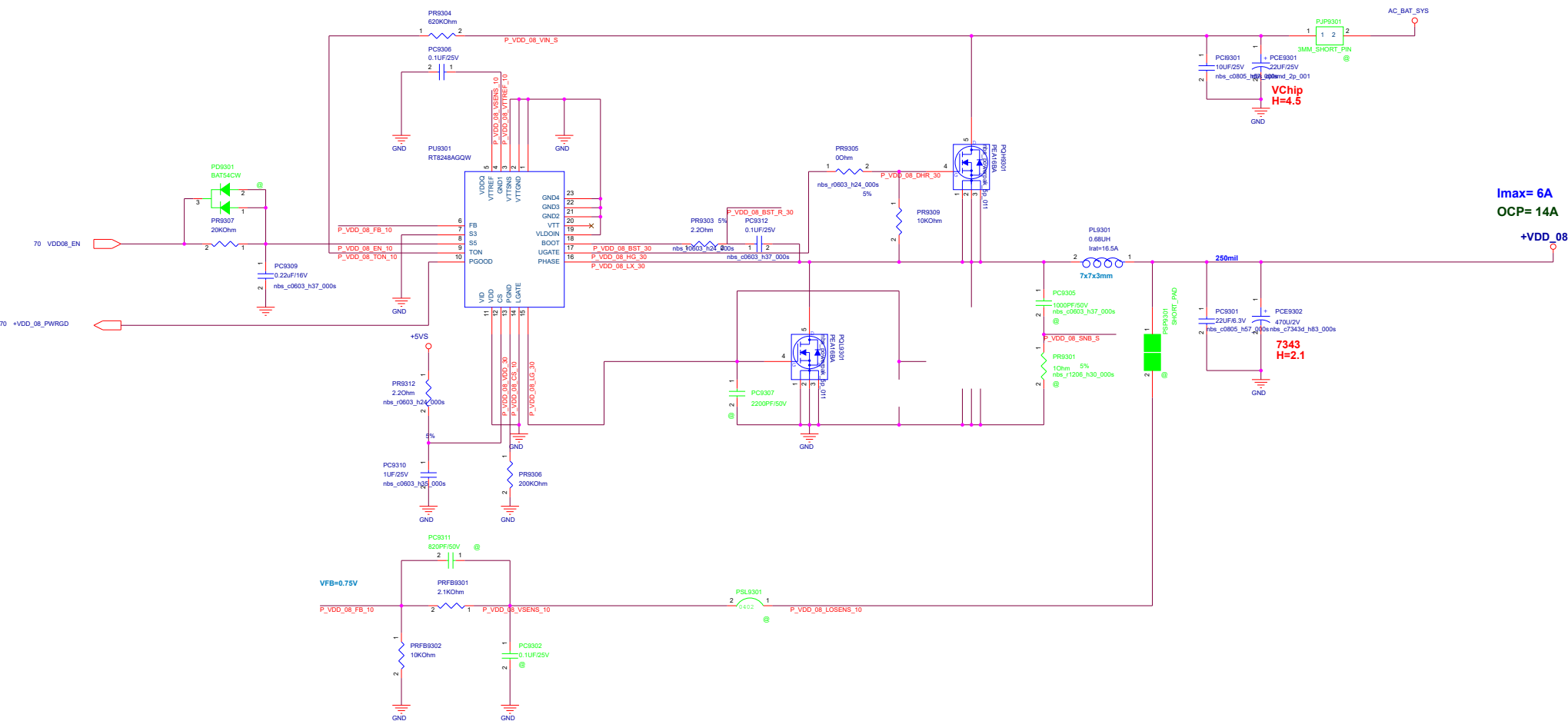
		Project Name GL7022C	Rev R1.0
Title : PW_+VMEMIO			
Size <i>Custom</i>	Dept.: NB Power team		Engineer: Joe
Date: Thursday, June 15, 2017		Sheet 94	of 102

		Project Name		Rev
		Q304UA		2.0
Title : POWER_+VGFX_CORE				
Size Custom	Dept.: ASUSTeK COMPUTER INC. Engineer: Kevin			
Date: Thursday, June 15, 2017			Sheet	95 of 105

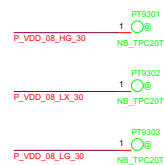




+VDD_08




PT830* 請放置 PU8301旁;並請放置Trace 上!

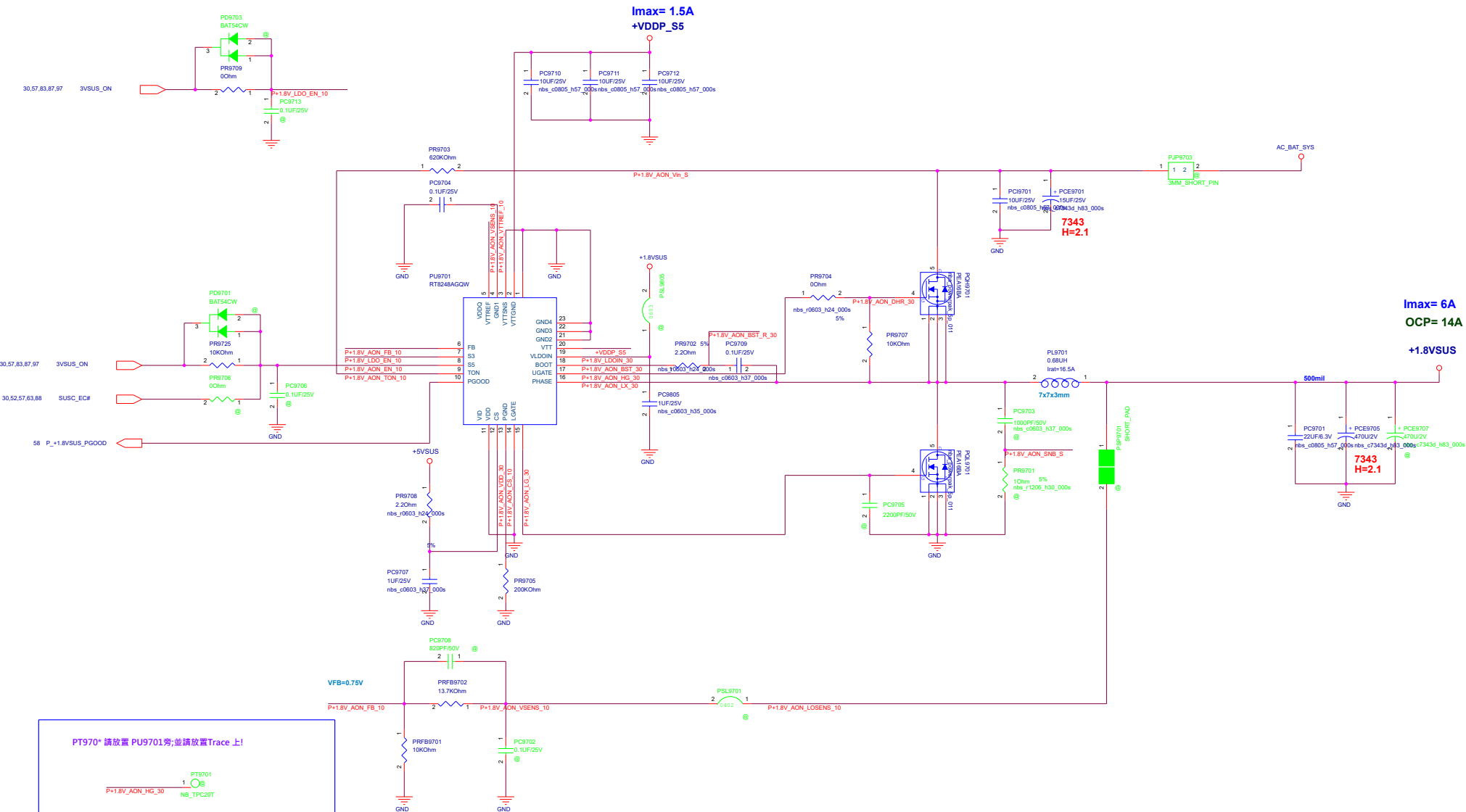


OCP= 2A



		Project Name		Rev	
		GL7022C		R1.0	
Title : PW_+12VS_FAN					
Size		Dept.: NB Power team		Engineer: Joe	
B					
Date: Thursday, June 15, 2017		Sheet		96 of 102	

+1.8V_CPU




PT970* 請放置 PU9701旁;並請放置Trace 上!

PT9701
1
P+1.8V_AON_HG_30
NB_TPC20T

PT9702
1
P+1.8V_AON_LX_30
NB TPC20T

P+1.8V_AON_LG_30

		Project Name		Rev
		Kabylake-H		R1.0
Title : PW_IPC				
Size Custom	Dept.: Power Team		Engineer:	Benson
Date: Thursday, June 15, 2017			Sheet	98 of 102